Design and Evaluation of a Fast, High-Resolution Sensor Evaluation Platform applied to MEMS Position Sensing

Lisa-Marie Faller, Tobias Mitterer, Juliana Padilha Leitzke and Hubert Zangl
Institute of Smart System Technologies
Sensors and Actuators
Alpen-Adria-Universität Klagenfurt
9020 Klagenfurt, Austria
Email: lisa-marie.faller@aau.at

Abstract

We present the design and implementation of an adaptable FPGA-based sensor evaluation platform. This platform is developed to benchmark a capacitive position sensor for a resonant micromirror system. The sensor is developed in a smart packaging solution as multilayer inkjet-printed electrode structure on a 3D-printed metal housing. Very high required resolutions of $res_{pos} < 50\,\mathrm{nm}$ together with a wide measurement range of $r_m = 1000\,\mu\mathrm{m}$ at an offset of $d_0 = 1000\,\mu\mathrm{m}$ motivate the development of such a platform. Still, it is fully adaptable to other sensing principles (e.g. inductive). The suggested platform provides high sampling rates (up to $\approx 10\,\mathrm{ns}$) and enables generation of trigger signals, i.e. the mirror control signal, without time lag (as could result from high order filters). The online configurable FPGA block structure in combination with host software blocks enables flexible and individual design. The sensor read-out circuitry is designed as carrier frequency system. Such a carrier frequency system enables flexible choices of bandwidth and measurement signal frequency. It thus allows for separation in frequency from coupling parasitics, i.e. other frequencies present in the device under test (e.g. actuation frequency in case of the micromirror system).

Index Terms

Capacitive sensors; Nanopositioning; Analog circuits; Digital signal processing; Sensor systems and applications; Demodulation.

I. Introduction

Often, the high requirements to measurement equipment lead to sophisticated customized solutions. These solutions are seldom generic enough to be applicable to others than the systems they were designed for. With the proposed measurement platform, we provide a highly sophisticated equipment in terms of bandwidth and resolution. Additionally, this platform is still flexible to be used in various system configurations and sensing applications.

The target application in this work is an inkjet-printed capacitive position sensor for a micro-optical device (or Micro Electro Mechanical System (MEMS)). Such micro-optical devices have been subject to increased interest over the last decade, and are nowadays employed in various fields. Applications range from Fourier Transform InfraRed (FTIR) spectroscopy [1] and multimedia devices [2], [3] to light barriers [4]. Previously, optical arrangements such as spectrometer devices, beamers, and others, used to consume a considerable amount of space. MEMS now offer the possibility to integrate complex setups into mobile applications. Advanced MEMS products are also appropriate to be used in lab-on-chip systems for space missions or Unmanned Aerial Vehicle (UAV)-based analyses.

The considered mirrors (Fig.1) are electrostatically driven at their mechanical resonance frequency, and are perfectly suitable for an application in FTIR spectrometers. In such a system, these devices are subject to concise demands regarding their performance: it is necessary to keep the measurement time low and provide a sufficient Signal to Noise Ratio (SNR). Thus, fast and accurate tracking of the mirror position is required.

Comparisons of interferometric and capacitive measurements on MEMS [5] have demonstrated advantages of optical measurements for characterization. Adversely, these measurement setups are not suitable for integration into the desired package outlines [6]. A multilayer, inkjet-printed, capacitive position sensor is considered here to enable further miniaturization.

A considerable amount of literature is available concerning capacitive sensors and their interface electronics: In [7]–[9], the authors pursue a strategy of directly connecting the capacitance of interest to a microcontroller. Energy-efficiency of capacitance sensor interfaces is addressed in [10] and [11]. The necessity to provide a fast read-out is also addressed (e.g. [12]–[14]). Capacitive sensing itself has been shown to be suitable for nanometer position resolution (e.g. [15]) and is advantageous due to low costs, and high resolution and bandwidth capabilities [16]. The capacitive sensor is manufactured as flat electrode structure. It then forms a parallel plate capacitor with the mirror plane, which is a common setup for nanometer applications [17]. The sensor is thus comparatively simpler to realize and integrate into an existing package. A capacitive sensor, manufactured by

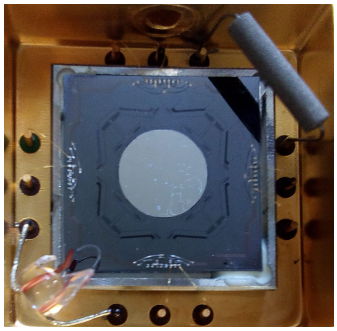


Fig. 1: MEMS mirror in vacuum capable brass package. The mirror is the lighter reflecting surface in the middle. It has a diameter of $d_{mir} = 5\,\mathrm{mm}$. An ion getter (upper right corner) is used to improve the vacuum, and a Pirani sensor (lower left corner) is employed to determine the vacuum quality.

such a rapid-prototyping technology, further is beneficial, compared to other manufacturing strategies (e.g. [18]–[20]), since this technology enables individual designs and can be applied to various setups.

In the remaining Subsections of Sec. I, related work and the comparison with other, commercially available products, is presented in Subsec. I-A. Then, our contribution is outlined in Subsec. I-B. In Sec. II, the mirror (Subsec. II-A) and the sensor design and integration (Subsec. II-B) are illustrated, followed by the interferometer principle in Subsec. II-C and discussions on the generations of interferograms in Subsec. II-D. Then, consequences of system deficiencies and measurement inaccuracies are illustrated for the FTIR system in Subsec. II-E. In Sec. III, capacitive sensing, the respective Finite Element Method (FEM) simulations and the carrier frequency setup are described. Afterwards, in Sec. IV, details on the analog design and hardware are presented. In Sec. V, we present a hardware-based noise analysis. Then, the respective sensor model is developed together with a subsequent determination of the parametric Cramer Rao Lower Bound (CRLB), i.e. the lower bound on the measurement variance. In Sec. VI, the developed digital signal processing blocks and wiring are illustrated. Then, Sec. VII presents the obtained measurement results for experimental determination of the hardware noise in the first place and the demodulation setup in the following. Finally, the conclusion is given in Sec. VIII.

A. Related Work

The read-out of capacitive sensors is commonly done using, e.g., Capacitance to Digital Converters (CDCs). Improvements on CDCs have been presented in, e.g., [21], [22], and [23]. Commercially available CDCs provide, e.g., $res_{pos} = 100\,\mathrm{nm}$ equivalent position resolution at an update rate of $f_s = 90\,\mathrm{Hz}$ [24]. Off-the-shelf systems are also available: Among others, the capaNCDT by $\mu\epsilon$ [25] provides $res_{pos} = 40\,\mathrm{nm}$ and a maximum bandwidth of $B = 8.25\,\mathrm{kHz}$. The Microsense 8810 system [26] is capable of providing $res_{pos} = 5\,\mathrm{nm}$ and a maximum rate of $B = 1\,\mathrm{kHz}$. The D-510 system provided by Physical Instruments is only able to cope with a distance offset $d_0 = 750\,\mu\mathrm{m}$ and is thus not fully comparable. The Microsense, $\mu\epsilon$ and PI Systems are not integrable into the MEMS package outline. Measurement ranges and average sensor distances of the considered devices are also smaller than required. The aforementioned systems measure capacitance directly. Alternatively, capacitance measurements can also be performed using a shunt. This concept is used for the system we suggest, as well as in the HF2 by Zurich Instruments. The HF2 employs lock-in amplifiers to realize the amplification of the sensor signal. Though the HF2 is comparable in terms of bandwidth, the reported input referred noise figure of ($u_n = 5\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$) limits the position resolution to, in our setup, $res_{pos} = 120\,\mathrm{nm}$. A comparison of available devices (see also [27]) is provided in Fig. 2 with respective comparison metrics listed in Tab. I: to improve readability, the bandwidth of the target system in the illustration is lower ($B = 60\,\mathrm{kHz}$) than the true specified bandwidth of up to $B = 180\,\mathrm{MHz}$. Also for the HF2, the bandwidth in the illustration ($B = 20\,\mathrm{kHz}$) is lower than the true bandwidth of up to $B = 50\,\mathrm{MHz}$. Most of the presented systems available up to now, provide sufficiently low noise by considering small bandwidths. Systems operating at higher bandwidth suffer from higher measurement noise due to thermal noise power integrated over the considered bandwidth. Additionally, all of the presented systems lack the possibility to access and adapt the signal processing directly. Thus, the small necessary latency cannot be reached by any of those hardware platforms.

B. Contribution

To fill the gap in measurement systems, in this work, a high-end measurement platform is developed and characterized (compare also [30]). The suggested FPGA-based hardware platform [31] enables higher sampling rates through employment of high-speed ADCs (ADS62P48 by Texas Instruments) and intelligent signal processing. The specifically designed analog circuitry, as daughterboard to the FPGA (Xilinx Kintex7-410T) system (see Fig.3a), provides ultra-low noise amplification and conditioning of the input signal. While the system outlines of the presented laboratory prototype are rather huge, the design

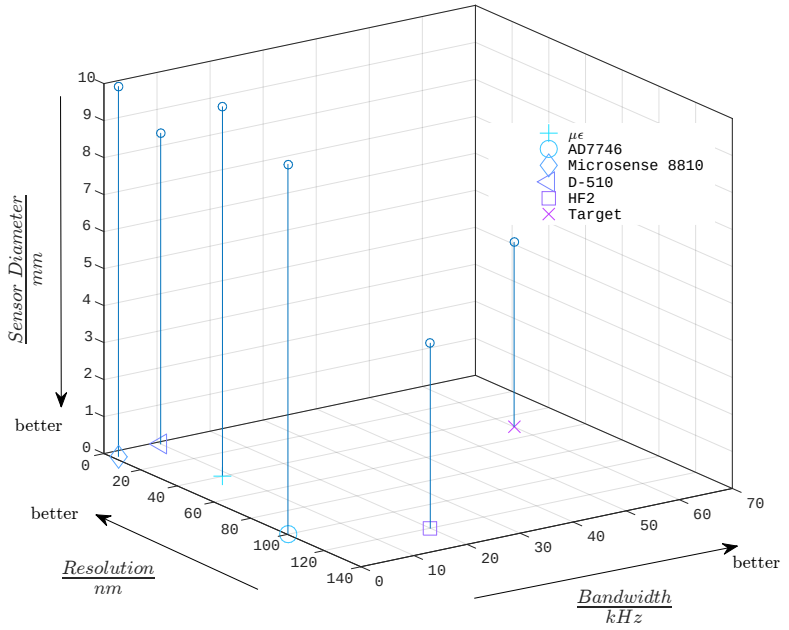
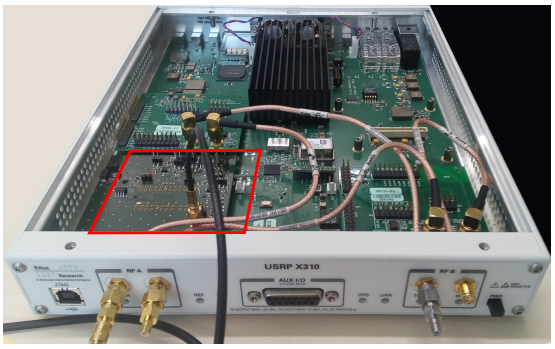


Fig. 2: Graphical comparison of available capacitive position sensing system and the suggested printed position sensor.

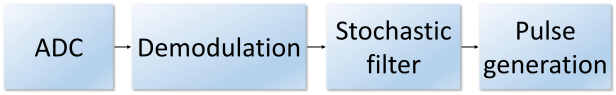
TABLE I: Table listing bandwidth and resolution specifications of commercially available capacitive position sensing systems. The Figure of Merit (FoM) for the considered systems is the achievable spectral distance noise. *Please note: the Microsense, $\mu\epsilon$ and PI Systems are not integrable into the optical MEMS package outline, also measurement ranges and average sensor distances of these devices are smaller than required.*

System	res_{pos}/nm	B/kHz	FoM/nm/$\sqrt{\text{Hz}}$	Provider
AD7746 [24]	100	0.09	10.54	Analog Devices
capaNCDT [25]	40	8.5	0.4339	$\mu\epsilon$
Microsense 8810 [26]	5	1	5	Microsense
D-510 PISeca [28]	2	10	0.02	Physical Instruments
HF 2 [29]	120	50×10^3	0.017	Zurich Instruments
this work	50	180×10^3	0.0112	

can be brought into an Application-Specific Integrated Circuit (ASIC) and can thus be miniaturized. The carrier frequency system as input circuitry, enables separation of the measurement- from other system frequencies, as well as a flexible choice of bandwidth (through, e.g., the choice of sampling frequency). This measurement setup is also suitable to be combined with other sensor effects (e.g. inductive). The provided underlying FPGA hard- and software-design are realized through individually adaptable blocks. It is thus possible to integrate customized hardware and software blocks (as shown in the blockdiagram in Fig. 3b). The final design will hold an Extended Kalman Filter (EKF) and a pulse generation block to control the excitation and processing of spectra for the micromirror (compare also [32]). The advantage of this structure is its online configuration ability: usually, FPGA (hardware) design is fixed by programming an image to the Flash memory of the device. The process of re-programming is rather time consuming since each time, the image has to go through routing, synthesis and implementation again. In the suggested system, the blocks realized in the FPGA can be parametrized at runtime. Additionally, also the block topology (connection) is reconfigurable without the necessity to rebuild the image.



(a) FPGA platform to be used with the specifically designed circuitry as well as the developed hardware design and software building blocks. Marked in red is the already attached daughterboard developed for this work.



(b) Blockdiagram showing the main blocks to be implemented and synthesized on the FPGA.

Fig. 3: FPGA hardware and target block architecture.

II. System Background

A. MEMS Mirror

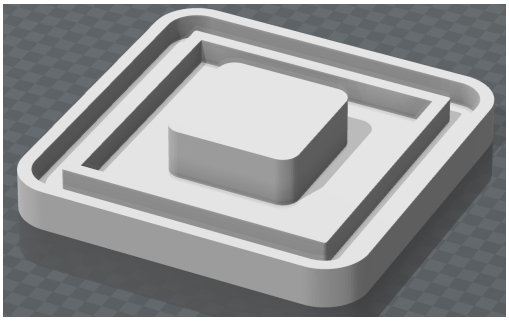
The considered measurement system application is position sensing and control of a MEMS mirror. This mirror is characterized with a resonance frequency of $f_{res} = 500\,\mathrm{Hz}$ achieving $s_{max} = 1\,\mathrm{mm}$ maximum stroke, or equivalently $s_{rel} = \pm 500\,\mu\mathrm{m}$ at a pressure below $P_{amb} = 50\,\mathrm{Pa}$ (vacuum). The mirror is suspended symmetrically on four pantographs and has an electrostatic drive excited by a Pulse Width Modulation (PWM) signal at twice the mirror resonance frequency, i.e. $f_{PWM} = 1000\,\mathrm{Hz}$. The actuation control is designed to guarantee the largest possible mirror stroke. Since this mirror is part of a miniaturized FTIR, it is necessary to track the mirror movement accurately enough to satisfy the spectrometer resolution requirements, that is, providing a position resolution of $res_{pos} \approx 50\,\mathrm{nm}$. The specifications for this application are gathered in Tab. II.

TABLE II: Table listing specifications for the position measurement of the MEMS mirror.

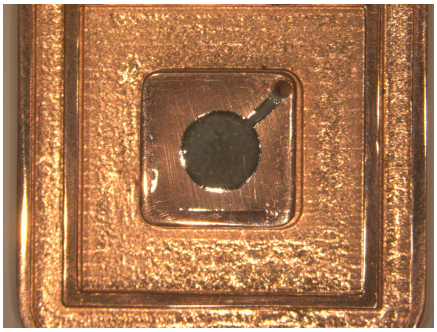
measurement range $r_m/\mu\mathrm{m}$	resolution res_{pos}/nm	bandwidth B/kHz	absolute error $e_{abs}/\%$
1000	50	20×10^3	< 2

B. Sensor Design and Integration

To integrate the sensor with the MEMS mirror, a functional 3D-printed copper housing (CAD design in Fig. 4a and 3D-printed copper housing as substrate for the inkjet-printed electrode in Fig. 4b) is developed. Functional because the copper housing is conductive and can thus be used as shielding which is necessary below the capacitive sensing electrode (dark circle and conductor path in Fig. 4b). The trench at the outside of the housing provides space for an O-ring to preserve the vacuum capabilities of the device. The housing and sensor can then be superposed to the mirror brass package shown in Fig. 1. The



(a) CAD drawing of the designed copper housing.



(b) Inkjet-printed electrode printed upon an isolation layer on the copper housing.

Fig. 4: Illustration of the design of the copper housing and the printed electrode.

inkjet-printing is done using a printer especially developed for research purposes, the PiXDRO LP50, Meyer Burger AG. This printer provides a dual-head assembly equipped with two identical inkjet print-heads (SM-128 Spectra S-class, Fujifilm Dimatix) with a $d_n = 50\mu m$ nozzle diameter and $s_d = 50pL$ calibrated drop size. The print-heads are capable of a maximal resolution of $res_{max} = 800\,\mathrm{dpi}$.

-First an insulating layer is printed to cover the copper at the center of the housing. The insulating, low-k dielectric ink is a mixture of acrylate-type monomers (Solsys EMD6200, SunChemical). The dielectric ink was jetted at a head temperature of $t_h = 50°C$ again without substrate table heating. In case of the insulating ink, substrate table heating does not provide any benefit, it rather destabilizes the printed layer: the insulating layer ablates under the influence of elevated temperatures. Then, conductive ink is printed to produce the electrode structure, and a conductor path which leads to a drill hole in the upper right corner, where the subsequent cable is to be connected.

The conductive ink is a nanoparticle silver (Ag) ink (Sycris I50DM-119, PV Nanocell) with 50 wt.% silver loading and average particle size of $s_p = 120\,\mathrm{nm}$ (d90). The silver ink was jetted at room temperature without heating of the substrate table. Drying the ink before photonic curing reduces the risk of outgassing. However, in this case, the silver ink is part of a multilayer structure. It is printed onto insulating ink which is not tolerant against elevated temperatures. Thus, substrate table heating is avoided. After each printing step, photonic curing using specially developed UV-curing equipment is done to finalize the printed structures.

C. Interferometer Principle

A common way to manufacture an FTIR spectrometer is the Michelson interferometer setup. The Michelson two-beam interferometer principle is not the only useful setup to build an interferometer. Other designs have been developed and proven more appropriate for certain measurements. Nevertheless, the interferometer design as suggested by Michelson in the middle of the 19th century still best illustrates the working principle. In such a setup, the spectrometer is composed of an IR-source

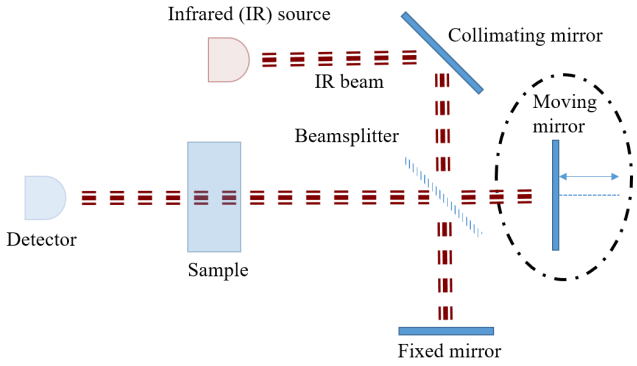


Fig. 5: Schematic illustration of the basic construction principle of a Michelson interferometer. The considered application in this work is position measurement of the moving mirror which is marked by the circle.

as well as a moving and a fixed mirror. The beam of an infrared light source is split among the two resulting paths. These two paths are of different length and consequently cause a phase shift of the electromagnetic vectors of the two light beams. At the subsequent recombination of these beams, interference occurs. The resulting amplitude then depends on the phase difference of the two beams. The light incident at the detector is then determined as a function of the path difference. In Fig. 5 the device is schematically illustrated: First, the collimating mirror collects and parellelizes the rays of the infrared light. Then, the beamsplitter, at the center of the apparatus, equally splits the incident light between the reference path (fixed mirror) and a path containing a mirror which moves perpendicular to the plane of incident light. The beams are reflected at the fixed and moving mirror surfaces and return to the beamsplitter. At the beamsplitter, both light beams interfere, yielding different intensities over all contained wavelength depending on the different pathlength travelled. Due to sample attributes at the molecular level, certain wavelength are absorbed more than others. The interaction of the resulting beam with the sample then holds the spectral information which is collected at the detector. After processing and Fourier transforming the data, a sample-characteristic spectrum can be seen.

One movement along the full possible pathlength the mirror can traverse, is called a scan. When the moving mirror is excited at constant velocity, the device is called a *continuous-scan* interferometer. Which is in contrast to *step-scan* interferometers which are equipped with stepwise moveable mirrors. *Rapid-scan* interferometers are a subclass of continuous-scan devices and rely on mirrors moving at velocities of $v_m > 10\,\mathrm{mm/s}$.

A characteristic property of such devices is the so-called *mutliplex advantage* [33]. It accounts for the fact that the SNR of these devices can be increased by an increased number of scans N as $SNR \propto N^{\frac{1}{2}}$. Disadvantageous at the same time is the increase of measurement time associated with this procedure.

Additional demands are: firstly, to add scans congruently, otherwise this results in a smeared result-spectrum; secondly, to provide low noise in the measured position: this blurs peaks and could thus lead to miss-identification of substances. Consequently, a concise knowledge of the mirror position during each scan is crucial.

D. Generation of an Interferogram

The determination of interferograms is based on interference of light, as mentioned previously. This may be best explained based on a simplistic example: consider monochromatic radiation, i.e., a *single wavelength light beam*, such as emitted by a laser. Let it be of wavelength λ_l: its wavenumber is then $W_l = 1/\lambda_l$. The intensity at W_l may be denoted by $I(W_l)$. Now, consider a continuous-scan interferometer which is, in the first place, at rest, when the both paths, the light travels, are of the same length. In other words, the Optical Path Difference (OPD) or retardation δ at this point is zero: the instrument is at Zero Path Difference (ZPD). The beams constructively interfere when recombined at the beamsplitter.

The maximum constructive interference is achieved at all path difference values where the positions of troughs and valleys of the vector signals overlap, i.e., there is no phase shift $\phi(\delta)$. This will be the case for all values where $\delta = n\lambda$ for any integer n, i.e., the OPD is an integral number multiple of the wavelength [34]. *Remark*: The OPD is twice the difference

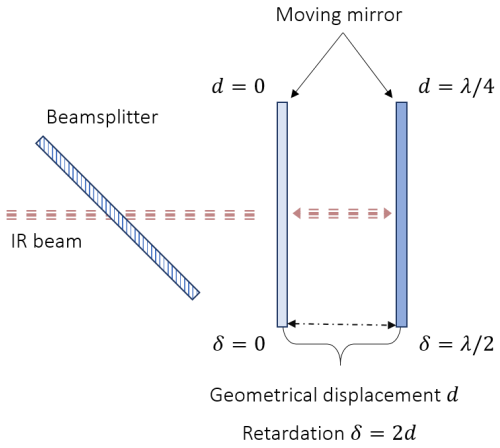


Fig. 6: Illustration of the mirror movement and respective geometrical displacement and beam retardation.

in geometrical pathlength d since the light travels back to the mirror, is reflected at the mirror surface and travels forth again until reaching the beamsplitter (see Fig. 6).

On the other hand, the more the location of troughs and valleys of the two beams drift apart, the smaller the resulting combined beam intensity becomes (see e.g. Fig. 7) until a minimum is reached at a phase shift of $\phi(\delta) = 180\,^\circ$ which occurs at an OPD of $\delta = \lambda/2$.

Commonly, the intensity is given as function of the retardation as

$$I(\delta) = \frac{I(W_s)}{2}\left(1 + cos\left(2\pi\frac{\delta}{\lambda_s}\right)\right) \tag{1}$$

where the letter s indicates the source quantities. The reading which holds the information is the dynamic component of the intensity (corresponding to the fraction of Eq. 1 multiplied to the cosine). The interferogram for the previously suggested laser source would thus read

$$I(\delta) = \frac{I(W_l)}{2}cos(2\pi W_l\delta) \tag{2}$$

To generally determine a proper interferogram, reflecting only sample properties, and not instrument characteristics, it is necessary to introduce a function to compensate for instrument deficiencies. This function, in general, depends on the wavenumber. Finally, the AC output voltage giving the interferogram can be given by

$$V(\delta) = \mathrm{B}(W_s)cos(2\pi W_s\delta) \tag{3}$$

where $B(W_s)$ is called the single-beam spectral intensity and is characteristic of the respective instrument.

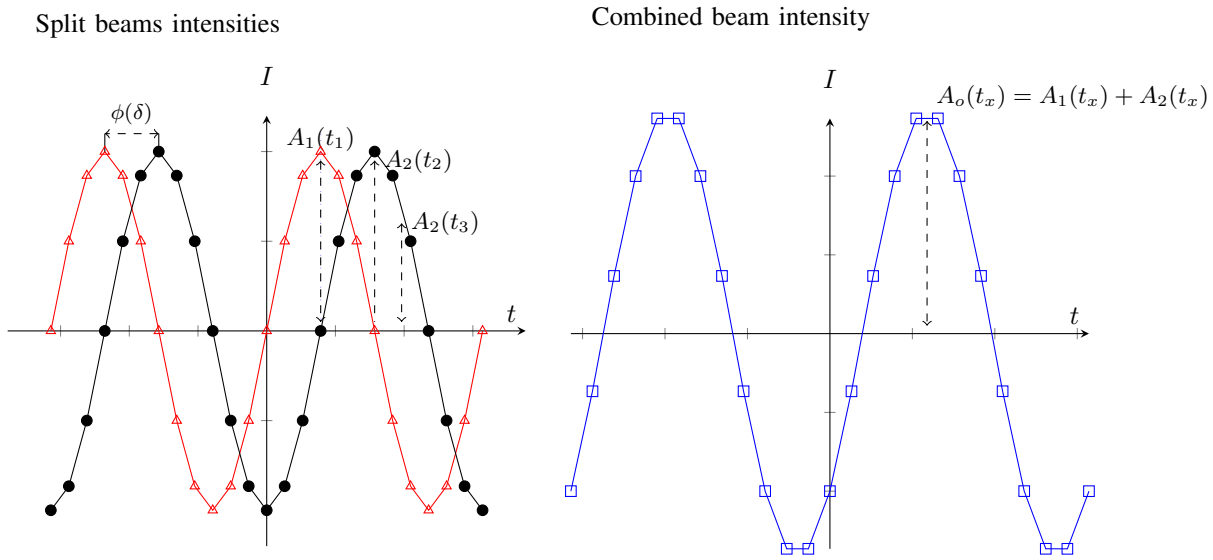


Fig. 7: Constructive interference at $\delta = \lambda/4$. The resulting intensity is the sum of both beams' intensities. Here, its maximum is less than at ZPD.

Having elaborated the intensity as a function of the cosine of the wavenumber, we can motivate the naming of the considered spectrometers, since $V(\delta) = \mathcal{F}(B(W_s))$ where $\mathcal{F}(\cdot)$ denotes the Fourier Transform (FT) operator. The output signal is the cosine Fourier Transform of the source single-beam intensity, mechanically performed through the mirror movement. The absorption spectrum can thus be determined based on an inverse Fourier Transform of the output signal.

-When the source emits light at more than one wavenumber, the resulting interferogram is the combination of the respective sinusoids. While the interferogram in these cases is still sinusoidal, it exhibits an exponentially decaying amplitude, and the broader the source spectrum is, the smaller is the envelope of the resulting interferogram. For the transition to a continuous source, the interferogram is determined by the integral

$$V(\delta) = \int_{-\infty}^{\infty} B(W_s) cos(2\pi W_s \delta) dW_s \tag{4}$$

and the intensity is then

$$B(W_s) = \int_{-\infty}^{\infty} V(\delta) cos(2\pi W_s \delta) d\delta \tag{5}$$

Obviously (since mathematically, this is an integration over δ), the resolution of the respective spectrometer can be increased by increasing the achievable retardation. In theory, infinite resolution is thus possible (although for infinite retardation).

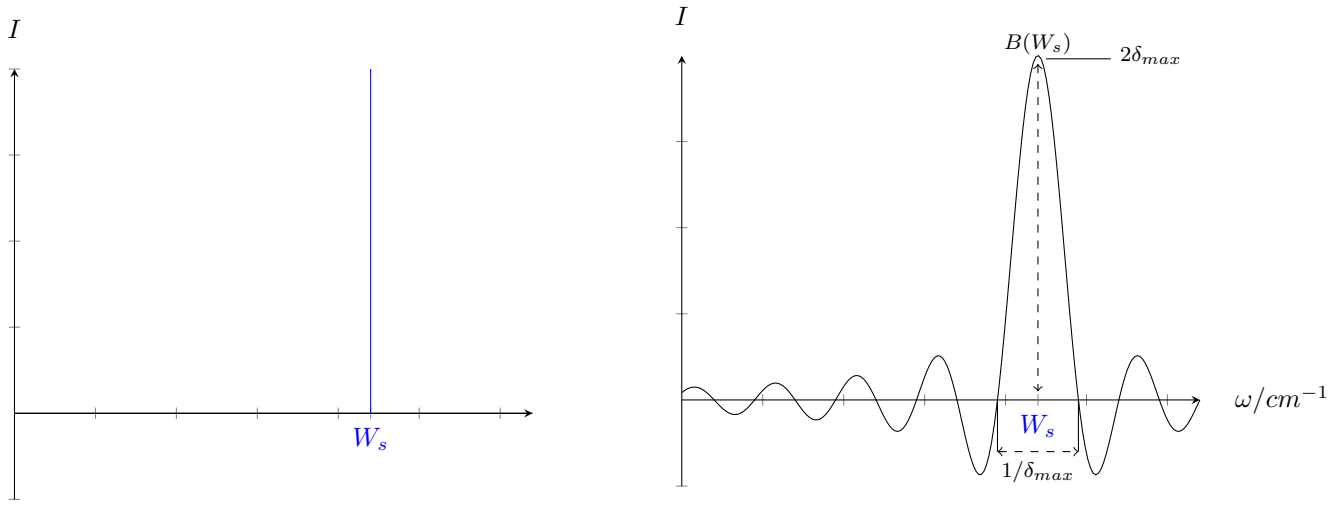
E. Consequences of Finite Retardation and Sensor Inaccuracy

Clearly, infinite retardation is not realizable physically and common spectrometers have a limited wavenumber resolution which is determined by [35]

$$res_W = \frac{1}{\delta_{max}} \tag{6}$$

In terms of the Fourier Transform this is equivalent to multiplying the true interferogram to a window function which truncates the reading to leave only values in the region $-\delta_{max} < \delta < \delta_{max}$. Such a truncation function $T(\delta)$ may be termed a *boxcar truncation function*. Thus, the intensity becomes

$$B(W_s) = \int_{-\infty}^{\infty} V(\delta) T(\delta) cos(2\pi W_s \delta) d\delta \tag{7}$$



(a) Spectrum of monochromatic light at wavenumber W_s.

(b) Interferogram of the monochromatic light at W_s as a result of the convolution with the instrument line shape function.

Fig. 8: Spectrum and resulting interferogram for monochromatic light.

It is well-known that multiplication in the time-domain is equivalent to a convolution in the frequency domain. That is to say, the resulting interferogram, mathematically is the convolution of the FT of the truncation function and the original spectrum. While the FT of the output signal $V(\delta)$ is the true spectrum $B(W_s)$, the FT of the truncation function is given by

$$\mathcal{F}(T(\delta)) = \tau(W_s) = 2\delta_{max}\frac{sin(2\pi W_s\delta_{max})}{2\pi W_s\delta_{max}} = 2\delta_{max}sinc(2\pi W_s\delta_{max}) \tag{8}$$

The convolution in the frequency domain is given as

$$C(W_s) = B(W_s) * \tau(W_s) = \int_{-\infty}^{\infty} B(\omega)\tau(W_s - \omega)d\omega \tag{9}$$

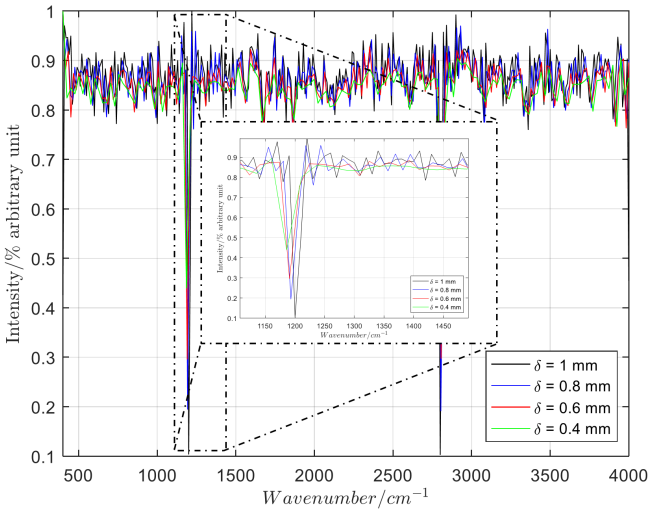
This function is called the Instrument Line Shape (ILS) function and is a characteristic of the respective instrument. The spectrum of a single wavenumber light and its resulting interference reading is illustrated in Fig. 8. To evaluate the influence of system variations on the resulting spectra, system simulations were done. A source, emitting homogenously with random fluctuations between $W_{s_{start}} = 400\,\mathrm{cm}^{-1}$ and $W_{s_{end}} = 4000\,\mathrm{cm}^{-1}$, and sample absorption peaks around $W_{a_1} = 1200cm^{-1}$ and $W_{a_2} = 2700cm^{-1}$ were generated. First, to evaluate the consequences of the achievable retardation of $\delta_{MEMS} = 1\,\mathrm{mm}$ and deviations from that value. Second, to assess the influence of inaccuracies in the absolute position measurement. The results for different retardations are given in Fig. 9a. The larger the retardation is, the more points are contained in the backtransformed spectrum. Thus, also the wavenumber resolution is increased with increasing retardation.

Evaluations of the consequences of absolute sensor measurement accuracy are illustrated in Fig. 9b. These evaluations show that the whole spectrum is compressed and the absorption peaks are moved along the wavenumber axis. It is thus important, to keep such an error as small as possible. If the sensor system is subject to such an inaccuracy, this can be compensated through calibration of the instrument using a known well-defined light source.

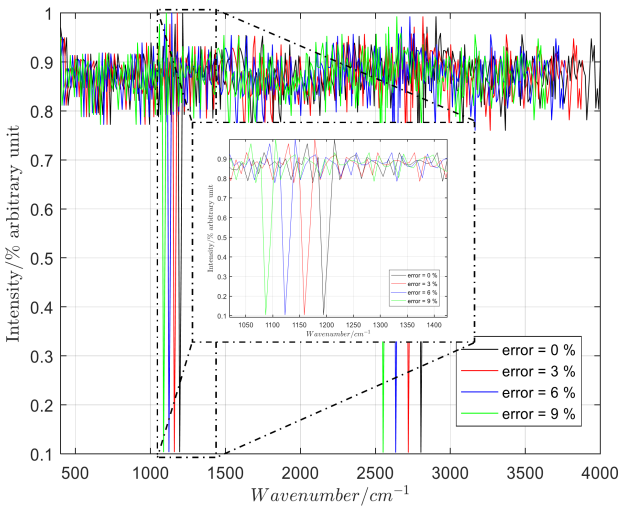
III. Capacitive Sensing and Measurement Circuitry

A micro-manufactured capacitive sensor is developed as multilayer structure at $d_0 = 1\,\mathrm{mm}$ below the mirror plate. This design comes with the advantage of being slim and readily integrable while providing for high resolution measurement capabilities (compare [36], [37]).

Capacitive sensors can be designed to work in either single-ended or differential mode. In both modes, the change in capacitance between conductive surfaces (electrodes), at different electric potentials, is measured. Applying a voltage at one electrode, consequently called transmitter, and measuring the resulting displacement current in a second electrode, i.e. the receiver, is termed differential mode. In a single-ended design, the displacement current at the transmitter is determined. Measurements in single-ended mode are possible to the open environment or distant ground.



(a) Simulation results for four different retardations: $\delta = 0.4{-}1\,\mathrm{mm}$.



(b) Simulation results for consequences of error in absolute measurement accuracy of the sensor.

Fig. 9: Illustration of consequences of system deficiencies.

In the target design, the bottom electrode is used as transmitter while the mirror incorporates the receiver. The electrode together with the mirror, are then assumed to form a structure resembling a parallel plate capacitor. In a simplifying approach, this can be approximated by the following model

$$C = \frac{\epsilon_0 \epsilon_r A_r}{d} \tag{10}$$

In Eq. 10, C is the capacitance in farads, A_r the active plate area in square meters, ϵ_0 the dielectric constant of vacuum, ϵ_r the relative dielectric constant of the material between the plates and d the plate spacing in meters. We consider an inkjet-printed sensor front-end employing single-ended, or self-capacitance measurement mode [38] which offers, in this case, better SNR than a differential system. Eq. 10 presents a simplistic approach, mainly usable to aid a basic understanding of the system. Accurate FEM simulations (compare also [39]) are set up to consider all effective influences (e.g. fringing fields etc.). In Fig. 10a, a simplified simulation setup is shown: The electrostatic field evolution is illustrated as coloured tubes emanating from the sensing electrode surface (red) and terminating at the mirror plane (blue). In Fig. 10b, the relationship of capacitance over time is illustrated: The label indicates the capacitance at the mirror rest position. The mirror movement is implemented by a moving mesh feature. The movement of the geometry is known, so the displacement of the mesh can be calculated at every time step using e.g. a Laplace smoothing approach. For the Laplace smoothing, it is necessary to solve the partial differential equation

$$\frac{\partial^2 x}{\partial X^2} + \frac{\partial^2 y}{\partial Y^2} + \frac{\partial^2 z}{\partial Z^2} = 0 \tag{11}$$

The lowercase letters are deformed mesh positions and uppercase letters describe the undeformed positions [40]. After the mesh deformation is determined, the electrostatics are computed by solving Gauss law

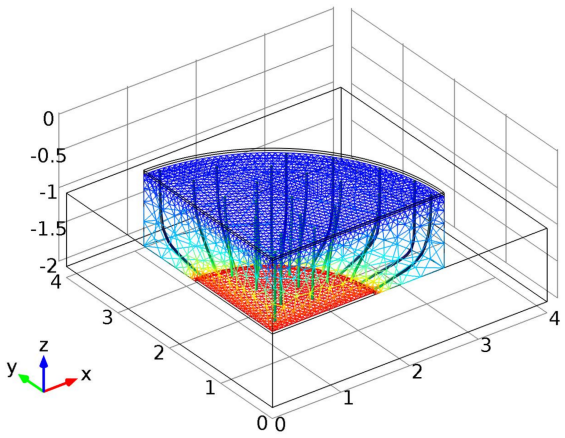
$$\nabla D = \rho_V \tag{12}$$

where the electric displacement field is

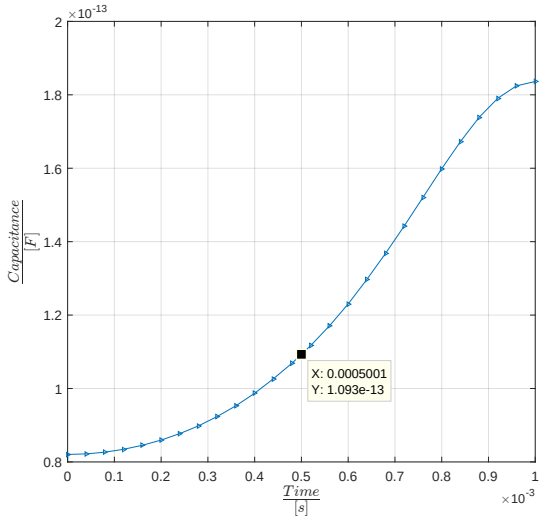
$$D = \epsilon_0 E \tag{13}$$

and ρ_V is the space charge density.

In the proposed carrier frequency system (compare [41], Fig. 11), the measurement capacitance is one component of a voltage divider with the second component being a $R_s = 50\,\Omega$ (R_{23} in Fig. 11) shunt resistor, which matches the impedance to the subsequent coaxial cable that connects to the downstream analog amplifier chain. This so-called power matching is done, to assure that all of the signal energy is transferred to the receiver. Without proper matching circuitry, the energy will be reflected on the transmission line.



(a) Simplified illustration of the FEM simulation setup for the capacitive position sensor. Axes are in mm.



(b) Capacitance over time as result of the FEM simulation setup for the capacitive position sensor. The label indicates the capacitance at the mirror rest position.

Fig. 10: Illustration of simulation setup and achievable capacitance change.

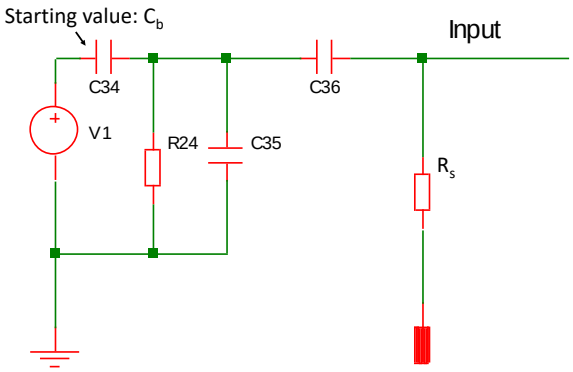


Fig. 11: Schematic illustration of the implemented setup, C_{34} is the capacitance of interest with a starting value of the sensor base capacitance C_b and $R_s = 50\,\Omega$ is the measurement shunt. R_{24} and C_{35} are parasitic parallel impedance and capacitance of the sensor to ground. C_{36} is the parasitic capacitance of the cable.

IV. Analog Design and Hardware

Commercially available hardware is not satisfying in terms of bandwidth and/or resolution. The suggested system therefore is comprised of an analog chain, attached as daughterboard to an FPGA.

The FPGA architecture is developed in distinct blocks, which are online configurable (after build) from a host, using a graphical interface. The architecture also provides the possibility to integrate customized hardware blocks in the FPGA image as well as software blocks in the open source host code.

The interface between analog and digital circuitry is realized through high speed, programmable gain ADCs providing a sample rate of up to $s_r = 180\,\mathrm{MHz}$ with a maximum of $res_{ADC} = 14\,\mathrm{bit}$ resolution. The sample rate and internal gain of these ADCs are not fixed, but can be chosen through the FPGA which is part of the provided flexibility of the presented system. A block diagram of the structure is provided in Fig. 12.

Fig. 12: Block diagram of the analog signal processing chain up to the high-speed ADCs.

The ADCs accept a differential signal of $v_{in_{pp}} = 2\,\mathrm{V}$ (where the subscript *pp* means peak-to-peak). To provide a well-conditioned signal to the ADCs, a specific amplifier chain (see Fig. 13) has been designed, realized as multistage structure of Low Noise Amplifiers (LNAs) with a device characteristic noise of $u_n = 1\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$. The first LNA stage has lower gain (≈ 10) than the second one (≈ 40). The relative noise contribution of the amplifier is more significant in the first stage, where the signal is smaller than in the second stage. Still, both amplifiers contribute to the overall noise and are considered in the design. To provide a suitable signal to the ADC, a signal reference conversion from single-ended to differential is

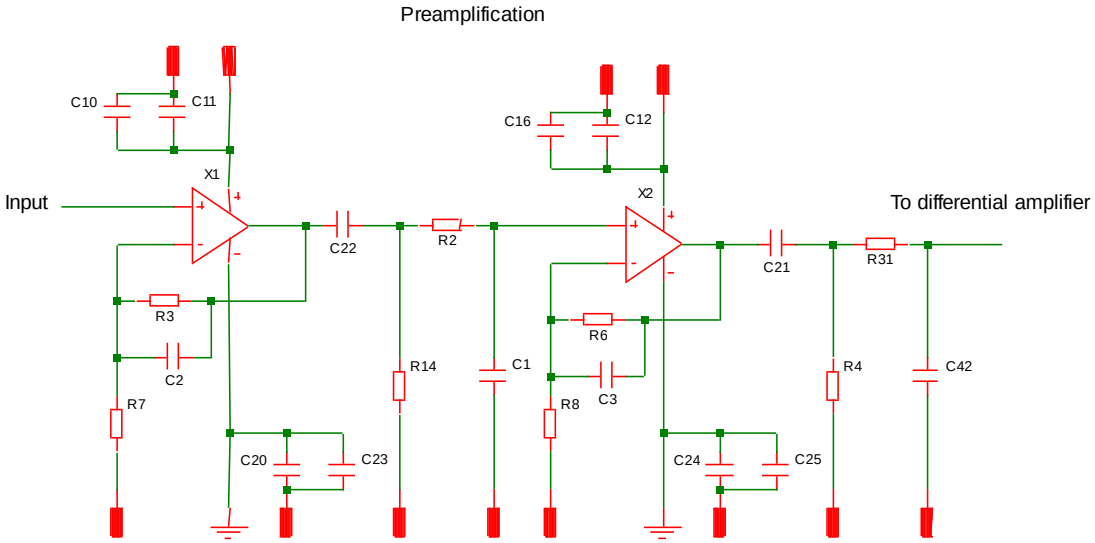


Fig. 13: Low-noise amplifier chain as implemented for signal conditioning. The feedback capacitors C_2 and C_3 are implemented to reduce peaking in the small signal frequency response. R_7 and R_8 together with the feedback resistors (parallel to C_2 and C_3) determine the gain. C_{22} and R_{14} as well as C_{21} and R_4 are used to block low frequencies as well as DC errors in the amplifier outputs. R_2 and C_1 and R_{31} and C_{42} are used for impedance matching of the connected stages. Other capacitors in the circuitry are implemented for voltage stabilization.

realized, using a differential amplifier circuit (see Fig. 14). Usually, such systems operate at high carrier frequencies, (e.g.,

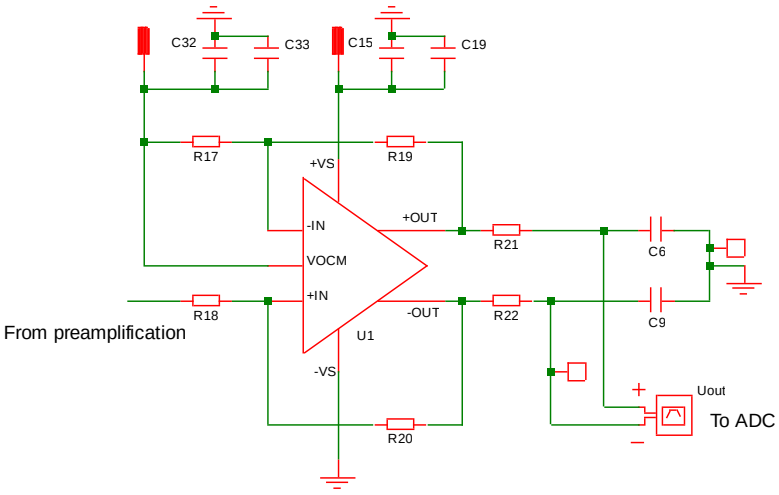


Fig. 14: Differential amplifier circuitry as realized to interface to the ADC. R_{17} and R_{18} together with R_{19} and R_{20} are used to set the gain of the amplifier. Through R_{21} and C_6 and R_{22} and C_9 a differential filter structure is realized to suit the switched capacitor inputs of the subsequent ADC.

$f_c = 10\,\mathrm{kHz}$-$1\,\mathrm{MHz}$) and low measurement bandwidth (max. $B = 6.25\,\mathrm{kHz}$) [42]. In contrast, the designed analog circuitry

has to provide ultra low noise over the whole useful system bandwidth, i.e. up to $B = 180\,\mathrm{MHz}$. In order to provide a more flexible signal conditioning, a programmable gain amplifier is also considered in the design.

V. System Analysis

In order to analyse the system capabilities in terms of uncertainty, it is necessary to determine basic noise figures inflicted by the underlying electronics. Experimental characterization of the LNA chain (see Sec. VII) yield a spectral input referred noise voltage of $U_n = 2.09\,\mathrm{nV}/\sqrt{Hz}$ at the measurement shunt. The sensor base capacitance is found from FEM simulations to be $C_b = 109.3\,\mathrm{fF}$ (C_{34} in Fig. 11). For further analyses, the capacitance equivalent noise $C_n = 0.151\,\mathrm{aF}\sqrt{Hz}$ is necessary. It can be found from

$$C_n = \frac{U_n}{\frac{\partial U_{out}}{\partial C}} \tag{14}$$

It is the ratio of the LNAs input referred noise voltage U_n, and the system's output voltage sensitivity to capacitance changes. This sensitivity of the output voltage at the shunt resistor is

$$\frac{\partial U_{out}}{\partial C} = \frac{U_{exc}}{8C_b^2 2\pi f_c(\frac{1}{R_s} + 8\pi C_p f_c)(\frac{1}{\frac{1}{R_s}+8\pi C_p f_c} + \frac{1}{8C_b\pi f_c})^2} \tag{15}$$

Here, an expression for U_{out} can be found, using basic formulae for voltage divider circuits, as

$$U_{out} = \frac{U_{exc} Z_p}{Z_p + (\frac{1}{j2\pi f_c C_b})} \tag{16}$$

The measurement system's equivalent parallel impedance is

$$Z_p = \frac{1}{\frac{1}{R_s} + j2\pi f_c C_p} \tag{17}$$

with the parasitic parallel capacitance $C_p = 100\,\mathrm{pF}$ included. These Equations are evaluated with a shunt resistor value $R_s = 50\,\Omega$ (R_{23} in Fig. 11), an AC excitation voltage $U_{exc} = 1\,\mathrm{V}$ and carrier frequency $f_c = 20\,\mathrm{MHz}$.

As shown in Sec. VII, the noise voltage at the ADC input is $\Delta U_{in_{eff}} = 1.78\,\mathrm{mV}$. The effective quantization noise voltage of the ADC can be determined as [43]

$$\Delta U_{q_{eff}} = \frac{Q}{\sqrt{12}} \tag{18}$$

where

$$Q = \frac{V_p}{2^{ENOB}} = \frac{1}{2^{11.4}} \tag{19}$$

where V_p is the peak voltage accepted at the ADC inputs and $ENOB$ the effective number of bits as given in the datasheet. We can find $\Delta U_{q_{eff}} = 0.106\,\mathrm{mV}$. Compared to the noise inflictions given by the amplifier chain and related devices, the quantization noise of the ADCs is here then $\approx 6\%$ of the integrated thermal noise and is thus not further considered.

We suggest the use of a calibration procedure to cope with variations in the base capacitance, uncertainties originating from topology deviations may then be neglected.

A. Sensor Model

In a first approach to a suitable semi-analytic model for the capacitive position sensor, a polynomial model is fitted to data from Finite Element Method (FEM) simulations. This is a commonly used process and well-documented in literature [16], [17].

We presume the behaviour of the measured signal (capacitance) $C(d_m)$ with d_m the parameter of interest, i.e. the mirror position or distance, to be analytically describable as (compare Eq. 10)

$$C(d_m) = \frac{\epsilon_0 \epsilon_r A_r}{d_m} \tag{20}$$

with the mirror position

$$d_m = d_0 + A_m cos(2\pi f_m t + \phi_m) \tag{21}$$

Here, $d_0 = 1\,\mathrm{mm}$ is the initial or rest position, $A_m = 0.5\,\mathrm{mm}$ the absolute maximal displacement or amplitude, $f_m = 500\,\mathrm{Hz}$ the mirror resonance frequency and ϕ_m the mirror phase.

While the analytic description, as given above, is a simplistic version of the true system behaviour, simulation data provides an improved description. Hence, an analytic expression for this data is sought, based on which further resolution capability analyses of the considered system are possible. With respect to the given preconditions, it is a viable procedure to employ a Least Squares Estimator (LSE) (compare e.g. [44]). The resulting semi-analytic description (metamodel) of the simulation data is then used to quantify necessary conditions on the system bandwidth, noise and hardware parameters to provide the necessary position resolution (see also [45])).

B. CRLB Analysis

In Eq. 21, three parameters, i.e. phase ϕ_m, amplitude A_m and the frequency component f_m are supposed to be subject to environmental influences and thus time-varying. Under these assumptions, we can find the CRLB, i.e. the lower bound on the variance, for the parameters with respect to a chosen carrier frequency and bandwidth. The CRLB for a signal $s(\theta)$ dependent on the parameter of interest θ embedded in AWGN is a special case of the general CRLB, and can be found from [44]

$$CRLB = \frac{\sigma^2}{\left(\frac{\partial s(\theta)}{\partial \theta}\right)^2} = \frac{\sigma^2}{\left(\frac{\partial C(d)}{\partial d}\right)^2} \tag{22}$$

The rightmost term is then the formulation adapted to our case. Analysing uncertainty evolution over bandwidth (Tab. III), we

TABLE III: Uncertainties for a parametric system description.

Parameter	Uncertainty	Unit
amplitude	13·73	nm
phase	$1{\cdot}1e^{-4}$	rad
offset	$4{\cdot}034e^{-5}$	nm
frequency	11·62	Hz

see that employing a parametric description, already yields a theoretical lower bound of the uncertainty of, e.g., $CRLB_A < 14\,\mathrm{nm}$ for the amplitude. Here, we rely on the fact that the estimator output sample rate, i.e. the rate at which the mirror position measurements are given, is fixed. Increasing the sample rate at the input thus does not affect the CRLB. The CRLB remains fixed since, although the increased bandwidth causes an increased noise figure, averaging can be done using the input samples taken in excess.

A direct measurement setup demands for intractable restrictions on the bandwidth, as we showed in [46]. We consequently suggest to employ a parameterized system model, exploiting prior knowledge. This enables us to adopt measurement strategies allowing for higher considered bandwidths. To realize such a strategy, we apply statistical methods, i.e. an EKF, which, in essence, is a Bayesian approach to signal reconstruction. The developed LSE is then used in the EKF to estimate the mirror position.

VI. Digital Signal Processing

The suggested FPGA-based hardware platform [31] enables higher sampling rates through employment of high-speed ADCs and intelligent signal processing. The underlying FPGA hardware- as well as host software-design is realized through blocks. FPGA-design is also called hardware-design since, usually, the programmed structure and behaviours are hardwired, i.e. realized in hardware and can not be changed after build. The speciality of the presented platform is now its flexibility: In the suggested system, the blocks realized in the FPGA can be parametrized at runtime. These blocks are individually adaptable and thus enable various system configurations without suffering from long compile times. Additionally, also the block connections are reconfigurable without the necessity to rebuild the image. It is thus possible to integrate and wire customized blocks in hardware (on the FPGA) as well as software (on the host computer). In Fig. 15 the necessary blocks for the basic sensor evaluation procedure are depicted. The first block on the left configures the receiver hardware (the designed analog front-end) of the FPGA. The following two blocks are necessary for Digital Down Conversion (DDC) and demodulation. Demodulation is done through the Digital Signal Processor (DSP) chains available on the FPGA using a CORDIC algorithm [47]. The receive and both *DDC* blocks are executed on the FPGA. The following block (*Copy*) is used to transfer the same data to two sinks which are run on the host computer. The upper *Time Sink* is used to show the time domain signal. The lower *Frequency Sink* gives an FFT of the received and demodulated signal.

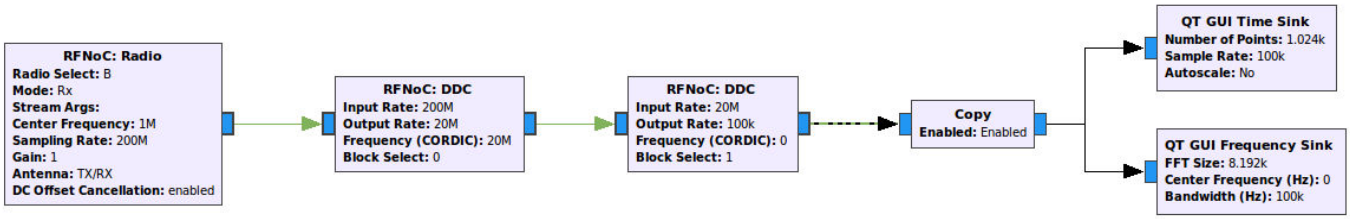


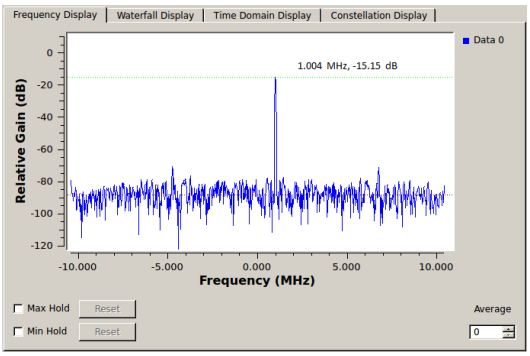
Fig. 15: Blockdiagram as used for sensor evaluation.

VII. Results

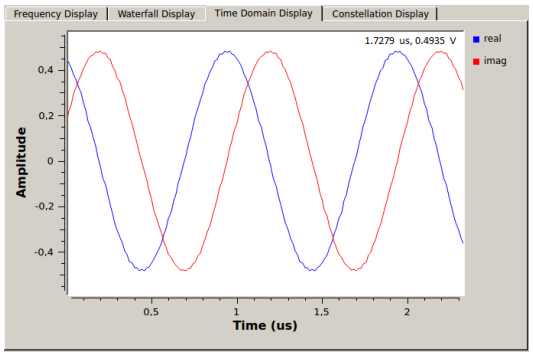
In the following, experimental evaluations of the hardware are presented. The result plots in the first two Subsec.s are given as originally retrieved on the considered measurement platform in order to illustrate also its visualization capabilities.

A. Hardware Noise Determination

To determine signal limitations of the analog design, we saturate the input amplifier chain to output the maximum value using a signal frequency of $f_{sig} = 1\,\mathrm{MHz}$. A Fast Fourier Transform (FFT) plot is given in Fig. 16a. Obviously, there are no disturbing harmonics yet when the analog chain is close to saturation. In Fig. 16b the respective time domain signal with maximum achievable amplitude is illustrated: The operation of the amplifier chain close to saturation leads to ripples at the upper and lower maximum of the sine curve. The signal is scaled to lie between $V_{scale} = \pm 0.5\,\mathrm{V}$ when transferred from the analog to the digital domain, the indicated achieved value of $V_{max} = 0.4995\,\mathrm{V}$ is thus close to the physical upper limit of the circuitry.



(a) FFT of an input signal with frequency $f_{sig} = 1\,\mathrm{MHz}$ (as indicated by the label).



(b) Time domain signal with frequency $f_{sig} = 1\,\mathrm{MHz}$ and maximum achievable amplitude (as indicated by the label).

Fig. 16: Visualization of FFT and time domain signals.

The noise evaluation is done for a sinusoidal input signal of $U_{in_{pp}} = 276\,\mathrm{mV_{pp}}$ or equivalently $U_{in_{eff}} = 95\,\mathrm{mV_{eff}}$ and a frequency of $f_{in} = 1\,\mathrm{MHz}$. A useful signal bandwidth of $B = 5\,\mathrm{MHz}$ is considered. The bandwidth-limitation is done for an upper corner frequency $f_{c_u} \approx 5.1\,\mathrm{MHz}$ by a high order digital filter, and for a lower corner frequency of $f_{c_l} \approx 10\,\mathrm{kHz}$ by the analog setup.

Comparing measurements of the voltage at the input and its digitized equivalent, the input-output relationship going from analog to digital domain can be found: a voltage of $u_{in} = 1\,\mathrm{mV}$ is mapped to a value of $u_{in_{dig}} = 0.001\,29$ in the digital domain.

Subsequently, a vector of the input signal $u_{in_{dig}}$ is recorded and subjected to an FFT. The useful signal (peak) in the FFT data is removed, to leave only noise in the spectrum. The resulting spectrum is then back-transformed (inverse FFT), yielding the noise voltage $u_{n_{out}} = 0.0023$, integrated over the used bandwidth $B = 5\,\mathrm{MHz}$. This is equivalent to a change in the effective input voltage of $\Delta U_{in_{eff}} = 1.78\,\mathrm{mV}$. To determine the noise figure Referred To the Input (RTI) $u_{n_{RTI}}$ in terms of $\mathrm{nV}/\sqrt{\mathrm{Hz}}$, it is necessary to divide $u_{n_{out}}$ by the circuit gain $G = 380$ and $\sqrt{B}$. Finally, a value of $u_{n_{RTI}} = 2.09\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$ can be found, which is in good accordance with the value of $u_{n_{sim}} = 1.75\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$ as was found in the simulation.

B. Sensor Evaluation Setup

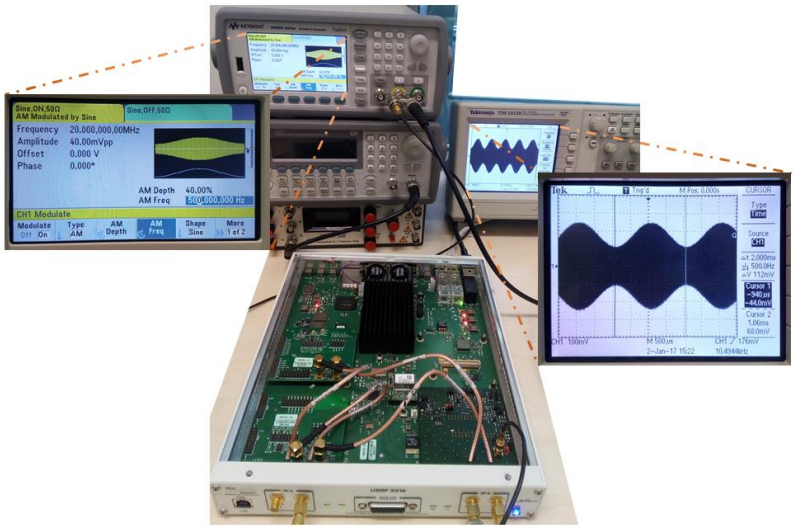


Fig. 17: Measurement setup using a signal generator (top left) providing the amplitude modulated signal and an oscilloscope (right) to validate the signal received by the FPGA platform (front).

When a sensor is connected to the carrier frequency setup as presented in Subsec. III, its measurement signal will be imposed on a carrier frequency by Amplitude Modulation (AM). The respective carrier frequency is, in general, free to choose, but depends on the environment in which the measurement takes place, type of sensor (e.g., capacitive or inductive) and required sampling rate.

To demonstrate the measurement capabilities of the presented system, the micromirror position measurement is considered. The measurement setup is illustrated in Fig. 17: A signal generator is used to provide the amplitude modulated signal. A signal with frequency $f_s = 500\,\mathrm{Hz}$ is imposed on a carrier frequency of $f_c = 20\,\mathrm{MHz}$. To assure proper operation of the signal generator, the AM signal is also coupled to an oscilloscope. On the FPGA measurement platform, the blockdiagram as given in Fig. 15 is run and the result as seen on the host computer is illustrated in Fig. 18. The upper graph of Fig. 18 illustrates the demodulated time domain signal with a frequency of $f_s = 500\,\mathrm{Hz}$, or equivalently, a period length of $t_p = 2\,\mathrm{ms}$. Below the time domain signal, an FFT plot is shown. In this plot, a peak at the carrier (at $f_{mid} = 0\,\mathrm{MHz}$) can be seen. Since the FFT produces a symmetric spectrum, two peaks of the AM signal can be seen at $f_{s+} = 500\,\mathrm{Hz}$ as well as $f_{s-} = -500\,\mathrm{Hz}$.

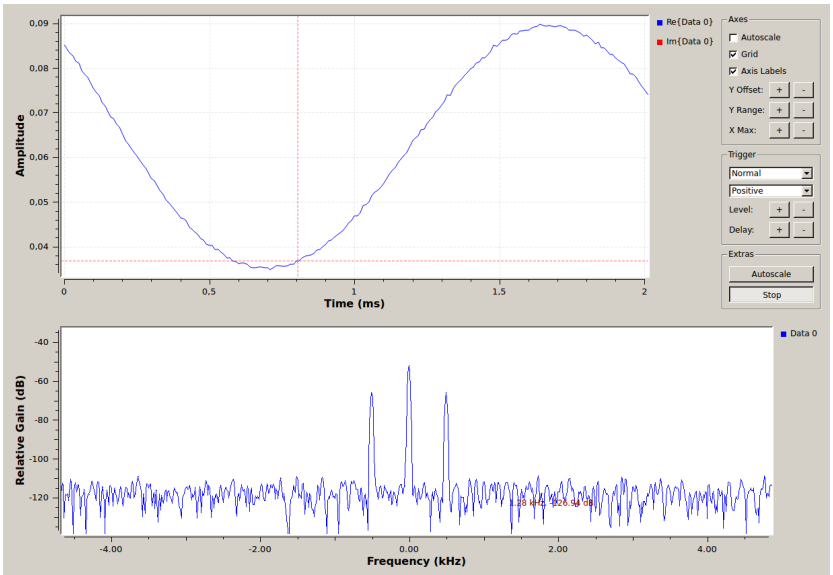


Fig. 18: Time domain signal with frequency $f_{sig} = 500\,\mathrm{MHz}$ in the upper graph and FFT of the received signal in the lower graph.

C. Frequency Plot

In order to determine the broadband suitability of the designed hardware, the frequency plot was determined over the whole frequency range of interest, going from $f_{min} \approx 10\,\mathrm{kHz}$ to $f_{max} \approx 100\,\mathrm{MHz}$. These measurements are done using a signal generator connected to the analog front-end. A frequency sweep signal is issued and the resulting output signal of the hardware is observed using a high resolution and high bandwidth oscilloscope. The cabling and connector influence was removed using a proper calibration procedure. The used oscilloscope input has lower bandwidth than the characterized hardware: Thus, the resolution bandwidth of the oscilloscope had to be adapted. The lower corner frequency is determined by the analog filter in the hardware design whereas the upper corner frequency is due to the frequency specifications of the used amplifiers and layout. The determined frequency range, this hardware is suitable for, is thus in good accordance with the requirements and specifications presented in Tab.I in Subsec.I-A at the beginning of this work.

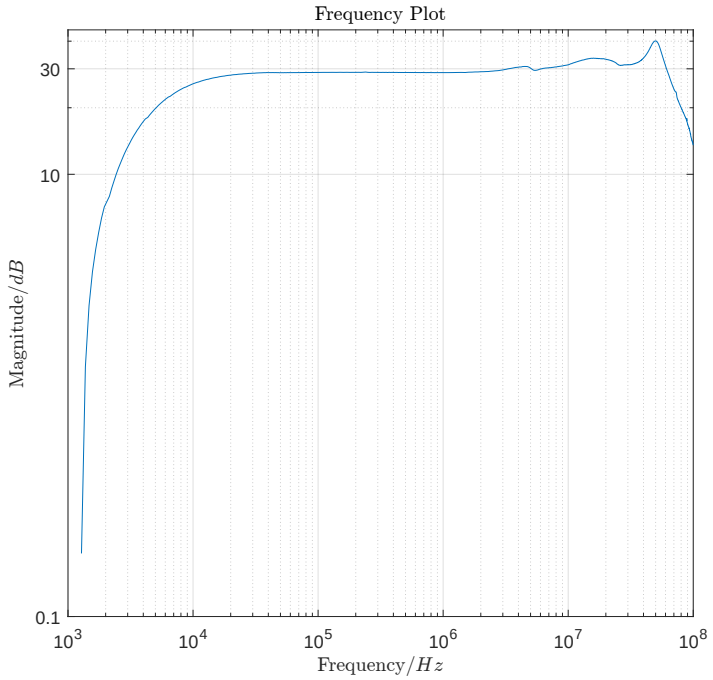


Fig. 19: Frequency plot illustrating gain versus frequency for the designed analog front-end.

VIII. Conclusion

In this work, design and implementation considerations for a sensor evaluation platform to be applied to a MEMS mirror system are presented. The considered hardware platform is introduced as consisting of an analog circuitry together with an FPGA and flexible signal processing software. The system is discussed giving details on the target MEMS mirror as well as an illustration of the 3D-printed copper housing and details on the inkjet-printing process to fabricate the capacitive sensor electrodes. Then, discussion of the interferometer principle, the generation of interferograms and effects of finite retardation and deficiencies in the sensor absolute accuracy are given. To illustrate the effects of such system deficiencies, simulations considering an IR broadband source with $W_s = 400 - 4000\,\mathrm{cm}^{-1}$ and two assumed sample absorption peaks are developed. The simulations are based on a mathematical description of the interferogram and its inverse FFT, yielding a result spectrum as the system output. Then, the FEM simulation setup and results for the nonlinear capacitance reading are detailed. Subsequently, the analog circuitry is presented based on detailed schematics of the carrier frequency input, the low noise amplifier chain and the differential amplifier as input to the ADCs. In the following, noise considerations are given for the developed system. Afterwards, digital signal processing to implement a demodulation scheme, applied to the micromirror position measurement, is illustrated. Noise evaluation measurement results, based on a measurement setup resembling the micromirror application, indicate that the designed analog front-end is suitable as low noise input circuitry. Demodulation measurements demonstrate the platform suitability for high resolution and high speed measurements using the suggested carrier frequency setup. It is shown that, with this system, a position resolution of $res_{pos} = 50\,\mathrm{nm}$ is possible at high bandwidths above $B = 10MHz$.

ACKNOWLEDGEMENT

This project has been supported by the COMET K1 ASSIC Austrian Smart Systems Integration Research Center. The COMET-Competence Centers for Excellent Technologies-Programme is supported by BMVIT, BMWFW and the federal provinces of Carinthia and Styria.

REFERENCES

[1] A. Tortschanoff, A. Kenda, M. Kraft, T. Sandner, H. Schenk, and W. Scherf, "Improved MOEMS-Based Ultra-Rapid Fourier Transform Infrared Spectrometer," in *Proc. SPIE, Next-Generation Spectroscopic Technologies II*, vol. 7319, 2009.

[2] A. Yalcinkaya, H. Urey, D. Brown, T. Montague, and R. Sprague, "Two-Axis Electromagnetic Microscanner for High Resolution Displays," *J. of Microelectromech. Syst.*, vol. 15, no. 4, pp. 786–794, August 2006.

[3] C. Winter, L. Fabre, F. Lo Conte, L. Kilcher, F. Kechana, N. Abel, and M. Kayal, "Micro-Beamer Based on MEMS Micro-Mirrors and Laser Light Source," in *Procedia Chemistry 1*, vol. 1311, 2006.

[4] A. Kenda, A. Frank, M. Kraft, A. Tortschanoff, T. Sandner, H. Schenk, and W. Scherf, "MOEMS-Based Scanning Light Barrier," *Procedia Chemistry*, vol. 1, no. 1, pp. 1299–1302, September 2009.

[5] V. Annovazzi-Lodi, S. Merlo, and M. Norgia, "Comparison of Capacitive and Feedback-Interferometric Measurement on MEMS," *J. of Microelectromech. Syst.*, vol. 10, no. 3, pp. 327–335, Sep. 2001.

[6] V. F.-G. Tseng, L. Wu, and H. Xie, "Inductive Eddy Current Sensing as a Displacement Sensing Mechanism For Large Piston/Rotation Micromirrors," in *IEEE Transducers*, 2015.

[7] F. Reverter and O. Casas, "Interfacing Differential Capacitive Sensors to Microcontroller: A Direct Approach," *IEEE Trans. on Instrumentation and Measurement*, vol. 59, no. 10, pp. 2763–2769, October 2010.

[8] O. Lopez-Lapeña, E. Serrano-Finetti, and O. Casas, "Calibration-less direct Capacitor-to-Microcontroller Interface," *IEEE Electronics Letters*, vol. 52, no. 4, pp. 289–291, February 2016.

[9] F. Reverter and O. Casas, "A Microcontroller-Based Interface Circuit for Lossy Capacitive Sensors," *Measurement Science and Technology*, vol. 21, no. 6, May 2010.

[10] H. Omran, M. Arsalan, and K. N. Salama, "An Integrated Energy-Efficient Capacitive Sensor Digital Interface Circuit," *Sensors and Actuators A: Physical*, vol. 216, pp. 43–51, September 2014.

[11] A. Alhoshany, H. Omran, and K. N. Salama, "A 45.8 fJ/Step, Energy-Efficient, Differential SAR Capacitance-to-Digital Converter for Capacitive Pressure Sensing," *Sensors and Actuators A: Physical*, vol. 245, pp. 10–18, july 2016.

[12] N. Libert, R. E. M. Morales, and M. J. Da Silva, "Capacitive measuring system for two-phase flow monitoring. part 1: Hardware design and evaluation," *Flow Measurement and Instrumentation*, vol. 47, pp. 90–99, March 2016.

[13] M. J. Da Silva, E. N. dos Santos, and T. P. Vendruscolo, "High-speed Multichannel Impedance Measuring System," *Acta IMEKO*, vol. 1, no. 1, pp. 36–41, July 2012.

[14] S. Thiele, M. J. Da Silva, and U. Hampel, "Capacitance Planar Array Sensor for Fast Multiphase Flow Imaging," *IEEE Sensors Journal*, vol. 9, no. 5, pp. 533–540, May 2009.

[15] J.-I. Lee, X. Huang, and P. B. Chu, "Nanoprecision MEMS Capacitive Sensor for Linear and Rotational Positioning," *J. of Microelectromech. Syst.*, vol. 18, no. 3, pp. 660–670, Jun. 2009.

[16] A. J. Fleming, "A Review of Nanometer Resolution Position Sensors: Operation and Performance," *Sensors and Actuators, A: Physical*, vol. 190, pp. 106–126, February 2013.

[17] T. Hicks and P. Atherton, *The NanoPositioning Book*. Queensgate Instruments Limited, 1997.

[18] S. I. Moore and S. O. R. Moheimani, "Displacement Measurement with a Self-Sensing MEMS Electrostatic Drive," *J. of Microelectromech. Syst.*, vol. 23, no. 3, pp. 511–513, Jun. 2014.

[19] M. S.-C. Lu and G. K. Fedder, "Position Control of Parallel-Plate Microactuators for Probe-Based Data Strorage," *J. of Microelectromech. Syst.*, vol. 13, no. 5, pp. 759–769, Oct. 2004.

[20] B. Cagdaser and B. E. Boser, "Low-Voltage Electrostatic Actuation With Inherent Position Feedback," *J. of Microelectromech. Syst.*, vol. 21, no. 5, pp. 1187–1196, Oct. 2012.

[21] V. Sreenath and B. George, "An Easy-to-Interface CDC WWith an Efficient Automatic Calibration," *IEEE Trans. on Instrumentation and Measurement*, vol. 65, no. 5, pp. 960–967, May 2016.

[22] P. Vooka and B. George, "An Improved Capacitance-to-Digital Converter for Leaky Capactive Sensors," *IEEE Sensors Journal*, vol. 15, no. 11, pp. 6238–6247, July 2015.

[23] B. George and V. J. Kumar, "Analysis of the Switched-Capacitor Dual-Slope Capacitance-to-Digital Converter," *IEEE Trans. on Instrumentation and Measurement*, vol. 59, no. 5, pp. 997–1006, May 2010.

[24] (2016, Feb.) Analog Devices. [Online]. Available: http://www.analog.com/media/en/technical-documentation/data-sheets/AD7745_7746.pdf

[25] (2016, June) Micro-Epsilon. [Online]. Available: http://www.micro-epsilon.com/displacement-position-sensors/capacitive-sensor/capaNCDT_6500/index.html

[26] (2016, June) MicroSense. [Online]. Available: http://www.microsense.net/products-position-sensors-microsense-8800.htm

[27] A. J. Fleming and K. K. Leang, *Design, Modeling and Control of Nanopositioning Systems*. Springer International Publishing Switzerland, 2014.

[28] (2016, June) Physical Instruments. [Online]. Available: https://www.physikinstrumente.com/en/products/sensors/capacitive-sensors/d-510-piseca-capacitive-sensors-500400/

[29] (2016, December) Zurich Instruments. [Online]. Available: http://www.zhinst.com/products?gclid=CPGRqcOgh9ECFRHgGwod8UYIYA

[30] L.-M. Faller and H. Zangl, "Design of a Fast, High-Resolution Sensor Evaluation Platform applied to a Capacitive Position Sensor for a Micromirror," in *Proc. of the IEEE I2MTC 2017*, 2017.

[31] (2016, November) Ettus Research. [Online]. Available: https://www.ettus.com/product/details/X310-KIT

[32] L.-M. Faller and H. Zangl, "Feasibility Considerations on an IInkjet-Printed Capacitive Postion Sensor for Electrostatically Actuated Resonant MEMS-Mirror Systems," *IEEE J. of Microelectromech. Systems*, no. 99, pp. 1–10, March 2017.

[33] B. C. Smith, *Fundamentals of Fourier Transform Infrared Spectroscopy*. CRC Press, 2011.

[34] P. R. Griffith and A. de Haseth, James, *Fourier Transform Infrared Spectroscopy*. John Wiley & Sons, 2007.

[35] P. R. Griffith, "Trading Rules in Infrared Fourier Transform Spectroscopy," *Anal. Chem.*, vol. 44, no. 11, pp. 1909–1913, September 1972.

[36] M. Carminati, G. Ferrari, F. Guagliardo, and M. Sampietro, "ZeptoFarad Capacitance Detection with a Miniaturized CMOS Current Front-End for Nanoscale Sensors," *Sensors and Actuators, A: Physical*, vol. 172, no. 1, pp. 117–123, December 2011.

[37] T. Zeng, Y. Lu, Y. Liu, H. Yang, Y. Bai, P. Hu, Z. Li, and J. Tan, "A Capacitive Sensor for the Measurement of Departure From the Vertical Movement," *IEEE Transactions on Instrumentation and Measurement*, vol. 65, no. 2, 2016.

[38] L. Baxter, *Capacitive Sensors, Design and Applications*. IEEE Press, 1997.

[39] L.-M. Faller and H. Zangl, "Robust Design of a 3D- and Inkjet-Printed Capacitive Force/Pressure Sensor," in *IEEE Proceedings of the EuroSimE 2016*, 2016.
[40] (2016, Feb.) Comsol multiphysics documentation, version 5.2.
[41] H. Zangl, "Design Paradigms for Robust Capacitive Sensors," Ph.D. dissertation, Techn. Univ. Graz, 2005.
[42] T. Schlegl and H. Zangl, "Sensor Interface for Multimodal Evaluation of Capacitive Sensors," *Journal of Physics Conference Series*, vol. 450, no. 1, 2013.
[43] A. Gersho, "Quantization," *IEEE Communications Society Magazine*, vol. 15, no. 5, pp. 16–29, September 1977.
[44] S. M. Kay, *Fundamentals of Statistical Signal Processing, Estimation Theory*. Prentice-Hall, Inc., 1993.
[45] L.-M. Faller and H. Zangl, "Robust Design of an Inkjet-Printed Capacitive Sensor for Position Tracking of a MOEMS-Mirror in a Michelson Interferometer Setup," in *Proc. of SPIE 10246*, 2017.
[46] ——, "Towards Feasibility of an Inkjet-Printed Capacitive Sensor for Position Tracking of a MOEMS-Mirror in a Michelson Interferometer Setup," in *Proceedings of the Eurosensors*, 2016.
[47] J. E. Valder, "The cordic trigonometric computing technique," *IRE Transactions on Electronic Computers*, vol. 8, no. 3, pp. 330–334, May 1959.