Design of a Fast, High-Resolution Sensor Evaluation Platform applied to a Capacitive Position Sensor for a Micromirror

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***Abstract*—We present the design and implementation of an adaptable FPGA-based sensor evaluation platform. This platform is developed for benchmarking of an inkjet-printed capacitive position sensor for a resonant micromirror system as part of a smart packaging solution. In the target system, very high required resolutions of $res_{pos} < 50\,\mathrm{nm}$ together with a wide measurement range of $r_m = 1000\,\mu\mathrm{m}$ at an offset of $d_0 = 1000\,\mu\mathrm{m}$ motivate the development of such a platform. Still, it is fully adaptable to other sensing principles (e.g. inductive). The suggested platform provides for high sampling rates (up to $\approx 10\,\mathrm{ns}$) and enables generation of trigger signals, i.e. the mirror control signal, without time lag (as could result from high order filters). The online configurable FPGA block structure in combination with host software blocks enables flexible and individual design. The sensor read-out circuitry is designed as carrier frequency system. Such a carrier frequency system enables flexible choices of bandwidth and measurement signal frequency. It thus allows for separation in frequency from coupling parasitics, i.e. other frequencies present in the device under test (e.g. actuation frequency in case of the micromirror system).**

***Index Terms*—Sensor Evaluation, FPGA, Carrier frequency system, Low noise amplifier, Noise analysis.**

I. Introduction

Often, the high requirements to measurement equipment lead to sophisticated customized solutions. These solutions are seldom generic enough to be applicable to others than the systems they were designed for. With the proposed measurement platform, we, on the one hand, provide for a highly sophisticated platform in terms of bandwidth and resolution. On the other hand, this platform still provides great flexibility to be used in varying system configurations and sensing applications.

The target application in this work is an inkjet-printed capacitive position sensor for a Micro-optical device (or MicroElectroMechanical Systems (MEMS)). Such MEMS devices enable development of new technologies and progress in various fields of industry as well as research.

The considered resonant, electrostatically driven mirrors, are perfectly suitable for application in Fourier Transform InfraRed (FTIR) spectrometers (compare [1]). In such a setup, those devices are subject to concise demands regarding their performance: it is necessary to keep the measurement time low and provide for a sufficient SNR. Thus, fast and accurate position tracking is required.

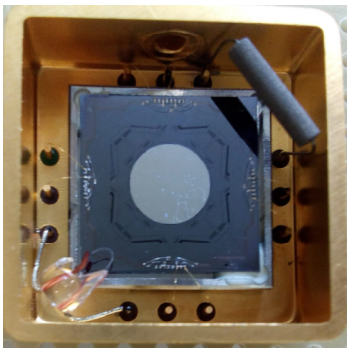

Fig. 1: MEMS mirror in vacuum capable package. The mirror is the lighter reflecting surface in the middle.

Comparisons of interferometric and capacitive measurements on MEMS [2] have demonstrated advantages of optical measurements for characterization. Adversely, these setups are not suitable for integration into desired package outlines [3]. Capacitive sensing, in contrast, has proven to be applicable for nanometer position resolution (e.g. [4]) and offers high resolution and bandwidth capabilities [5] at comparably low costs. The sensor is realized as flat electrode structure so as to form a parallel plate capacitor with the mirror plane, a setup which is also commonly used in nanometer applications [6]. Manufactured by inkjet-printing in a rapid-prototyping manner, it is beneficial compared to other capacitive sensing approaches (e.g. [7], [8] and [9]). It then enables adaptable designs and application to various setups.

In the MEMS mirror application, the presented sensor evaluation platform, enables further package miniaturization. However, its main advantage is that it facilitates the use of suboptimal, but highly flexible, sensor structures through the suggested combination of analog- and digital signal processing

hardware.

In the remaining Subsections of Sec. I, the mirror (Subsec. I-A) and interferometer principle (Subsec. I-B) are illustrated. The related work is presented in Subsec. I-C, and our contribution is outlined in Subsec. I-D. In Sec. II, capacitive sensing and the carrier frequency setup are described. Afterwards, in Sec. III, details on the analog design and hardware are presented. Sec. IV gives the respective noise analysis. Then, Sec. V presents the obtained measurement results. These are followed by the conclusion given in Sec. VI.

A. MEMS Mirror

The considered application is position sensing and control of a MEMS mirror. This mirror is characterized with a resonance frequency of $f_{res} = 500\,\mathrm{Hz}$ achieving $s_{max} = 1\,\mathrm{mm}$ maximum stroke, or equivalently $s_{rel} = \pm 500\,\mu\mathrm{m}$ at a pressure below $P_{amb} = 500\,\mathrm{Pa}$ (vacuum). The mirror is suspended symmetrically on four pantographs and has an electrostatic drive excited by a Pulse Width Modulation (PWM) signal at twice the mirror resonance frequency, i.e. $f_{PWM} = 1000\,\mathrm{Hz}$. The actuation control is laid out to guarantee for the largest possible mirror stroke. Since this mirror is part of a miniaturized FTIR, it is necessary to track the mirror movement accurately enough to satisfy the spectrometer resolution requirements, that is, providing a position resolution of $res_{pos} \approx 50\,\mathrm{nm}$.

B. Interferometer Principle

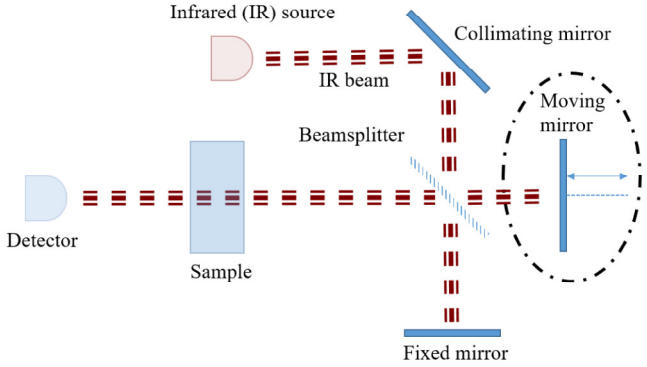

Fig. 2: Schematic illustration of the basic construction principle of a Michelson interferometer.

A common way to manufacture an FTIR spectrometer is a Michelson interferometer setup. In such a setup, the spectrometer is composed of an IR-source as well as a moving and a fixed mirror (Fig. 2). The IR light beam is split and, through interference, distinct wavelength of the IR light are selected dependent on the moving mirror position. The resulting monochromatic light beams pass through the sample of interest. Due to sample attributes at the molecular level, certain wavelength are absorbed more than others. Thus, different intensities at distinct wavelength can be seen at the detector. After processing and Fourier transforming the data, a sample-characteristic spectrum can be seen. One movement along the full possible pathlength the mirror can traverse, is called a scan. A characteristic property of those devices is the so-called *mutliplex advantage* [10]. It accounts for the fact that the Signal-to-Noise Ratio (SNR) of these devices can be increased by an increased number of scans (N) as $SNR \propto N^{\frac{1}{2}}$. Disadvantageous at the same time is the increase of measurement time associated with this procedure.

Additional demands are: firstly, to add scans congruently, otherwise this results in a smeared result-spectrum; secondly, to provide low noise in the measured position: this blurs peaks and could thus lead to miss-identification of substances. Consequently, a concise knowledge of the mirror position during each scan is crucial.

C. Related Work

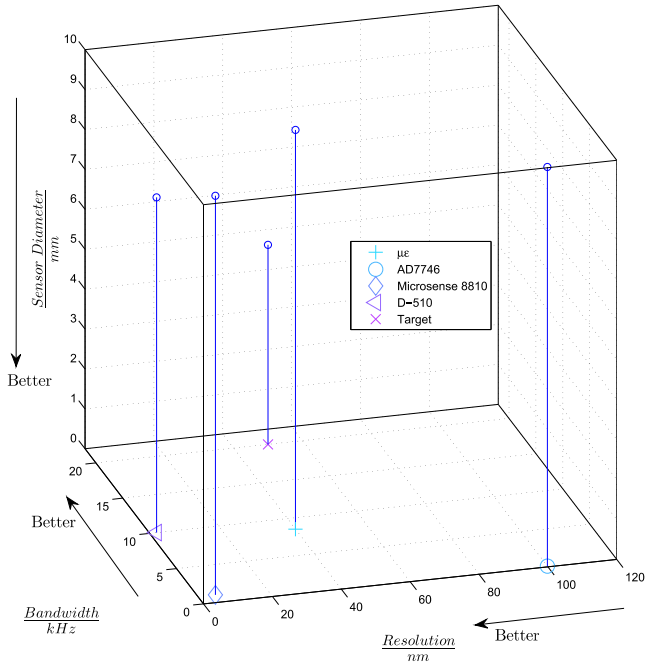

Fig. 3: Graphical comparison of available capacitive position sensing system and the suggested printed position sensor.

Commercially available Capacitance to Digital Converters (CDCs) provide for, e.g., $res_{pos} = 100\,\mathrm{nm}$ equivalent position resolution at an update rate of $f_s = 90\,\mathrm{Hz}$ [11]. Off-the-shelf systems are also available: Among others the capaNCDT by $\mu\epsilon$ [12] provides $res_{pos} = 40\,\mathrm{nm}$ and a bandwidth of $B = 8.25\,\mathrm{kHz}$, the Microsense 8810 system [13] is capable of providing $res_{pos} = 5\,\mathrm{nm}$ at a rate of $B = 1\,\mathrm{kHz}$. A comparison of available devices is provided in Fig. 3 with respective comparison metrics listed in Table I: due to reasons of readability, the bandwidth of the target system in the illustration is lower ($B = 20\,\mathrm{kHz}$) than the true specified bandwidth $B = 10\,\mathrm{MHz}$. The D-510 System provided by

Physical Instruments is only able to cope with a distance offset $d_0 = 750\,\mu\text{m}$ and is thus not fully comparable. The Microsense, $\mu\epsilon$ and PI Systems are not integrable into the MEMS package outline. Furthermore, measurements ranges and average sensor distances of the considered devices are smaller than required. All of the presented systems available up to now, provide sufficiently low noise by considering small bandwidths. Systems operating at higher bandwidths suffer from higher measurement noise due to thermal noise power, integrated over the considered bandwidth. Thus, existing devices can not be used for our application.

TABLE I: Table listing bandwidth and resolution specifications of commercially available capacitive position sensing systems. *Please note: the Microsense, $\mu\epsilon$ and PI Systems are not integrable into the optical MEMS package outline, also measurement ranges and average sensor distances of these devices are smaller than required.*

System	res_{pos}/nm	B/kHz	Provider
AD7746 [11]	100	0.09	Analog Devices
capaNCDT [12]	40	8.5	$\mu\epsilon$
Microsense 8810 [13]	5	1	Microsense
D-510 PISeca [14]	2	10	Physical Instruments

D. Contribution

The suggested FPGA-based hardware platform [15] enables higher sampling rates through employment of high-speed ADCs and intelligent signal processing. The specifically designed analog circuitry, as daughterboard to the FPGA system (see Fig.4), provides ultra-low noise amplification and conditioning of the input signal. The carrier frequency system as input circuitry, enables separation of the measurement-from other system frequencies, and flexible choice of bandwidth. The provided underlying hardware- as well as software-design is realized through individual blocks. These blocks are individually adaptable and thus provide flexible system configurations. It is thus possible to integrate customized hardware and software blocks (as shown in the blockdiagram in Fig.5). The final design will hold an Extended Kalman Filter (EKF) and a pulse generation block to control the excitation and processing of spectra for the micromirror. The advantage of this structure is its flexibility: usually, FPGA (hardware) design is fixed by burning an image to the device. In the suggested system, the blocks realized in the FPGA can be parametrized at runtime. Additionally, also the block topology (connection) is reconfigurable without the necessity to rebuild the image.

II. Capacitive Sensing and Measurement Circuitry

A micro-manufactured capacitive sensor is realized as multilayer structure at $d_0 = 1\,\text{mm}$ below the mirror plate. This design comes with the advantage of being slim and readily integrable while providing for high resolution measurement capabilities (compare [16], [17]).

Capacitive sensors can be designed to work in either single-ended or differential mode. In both modes, the change in capacitance between conductive surfaces (electrodes), at different electric potentials, is measured. Applying a voltage at one electrode, consequently called transmitter, and measuring the resulting displacement current in a second electrode, i.e. the receiver, is termed differential mode. In a single-ended design, the displacement current at the transmitter is determined. Measurements in single-ended mode are possible to the open environment or distant ground.

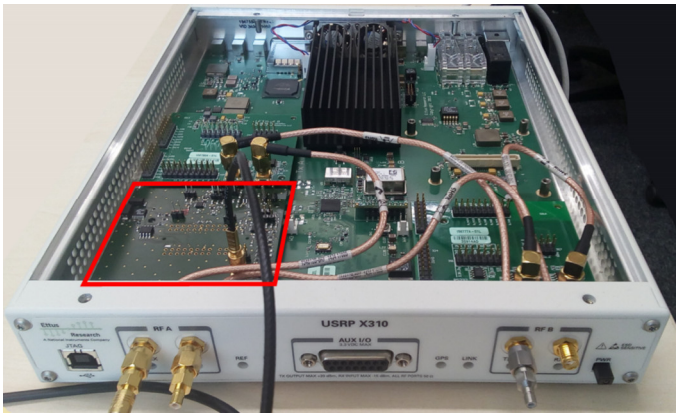

Fig. 4: FPGA platform to be used with specifically designed circuitry as well as developed hardware design and software building blocks. Marked in red is the already attached daughterboard developed for this work.

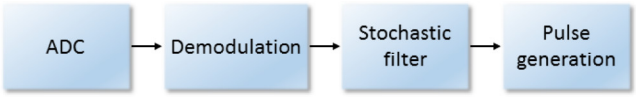

Fig. 5: Blockdiagram showing the main blocks to be implemented and synthesized on the FPGA.

In the target design, the bottom electrode is used as transmitter while the mirror incorporates the receiver. Both, the electrode as well as the mirror, are assumed to form a structure resembling a parallel plate capacitor. In a simplifying approach, this can be approximated by the following model

$$C = \frac{\epsilon_0 \epsilon_r A_r}{d} \tag{1}$$

In Eq. 1, C is the capacitance in farads, A_r the active plate area in square meters, ϵ_0 the dielectric constant of vacuum, ϵ_r the relative dielectric constant of the material between the plates and d the plate spacing in meters. We consider an inkjet-printed sensor front-end employing single-ended, or self-capacitance measurement mode [18] which offers, in this case, better SNR than a differential system.

In the proposed carrier frequency system (compare [19], Fig. 6), the measurement capacitance is one component of a voltage divider with the second component being a $R_s = 50\,\Omega$ shunt resistor, matching signal power to the subsequent coaxial cable that connects to the downstream analog amplifier chain. The power matching is done, to assure that all of the signal energy is transferred to the receiver. Without proper matching

circuitry, the energy will be reflected on the transmission line.

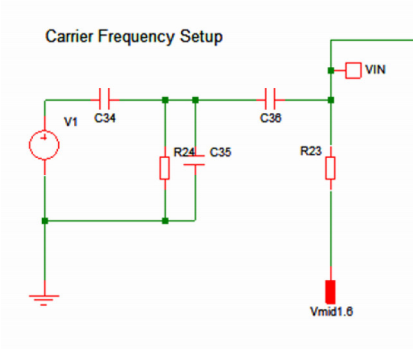

Fig. 6: Schematic illustration of the implemented setup, C_{34} is the capacitance of interest and R_{23} is the measurement shunt of $R_s = 50\,\Omega$.

III. Analog Design and Hardware

Commercially available hardware is not satisfying in terms of bandwidth and/or resolution. The suggested system therefore is comprised of an analog chain, attached as daughterboard to an FPGA.

The FPGA architecture is developed in distinct blocks, which are online configurable (after build) from a host, using a graphical interface. The architecture also provides the possibility to integrate customized hardware blocks in the FPGA image as well as software blocks in the open source host code.

The interface between analog and digital circuitry is realized through high speed, programmable gain ADCs providing a sample rate of up to $s_r = 180\,\mathrm{MHz}$ with a maximum of $res_{ADC} = 14\,\mathrm{bit}$ resolution. A block diagram of the structure is provided in Fig. 7.

Fig. 7: Block diagram of the analog signal processing chain up to the high-speed ADCs.

The ADCs accept a differential signal of $v_{in} = 2\,\mathrm{V_{pp}}$ (where the subscript *pp* means peak-to-peak). To provide a well-conditioned signal to the ADCs, a delicate amplifier chain (see Fig. 8) has been designed, realized as multistage structure of Low Noise Amplifiers (LNAs) with a device characteristic noise of $u_n = 1\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$. The first LNA stage has a significantly lower gain (≈ 10) than the second one (≈ 40) to avoid amplification of input-related noise. To provide a suitable signal to the ADC, a signal reference conversion from single-ended to differential is realized, using a differential amplifier circuit (see Fig. reffig:diff). Usually such systems operate at high carrier frequencies, (e.g., $f_c = 10\,\mathrm{kHz}$-$1\,\mathrm{MHz}$) and low measurement bandwidth (max. $B = 6.25\,\mathrm{kHz}$) [20].

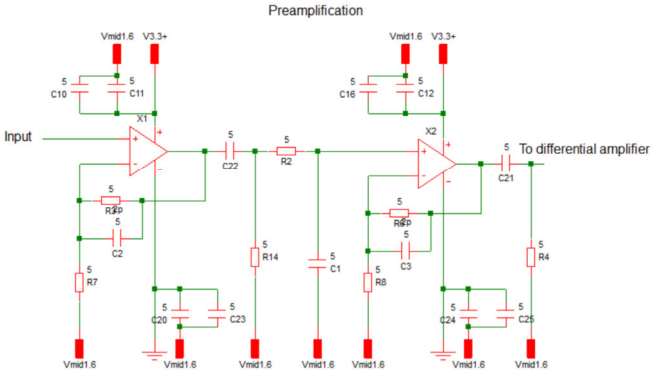

Fig. 8: Low-noise amplifier chain as implemented for signal conditioning.

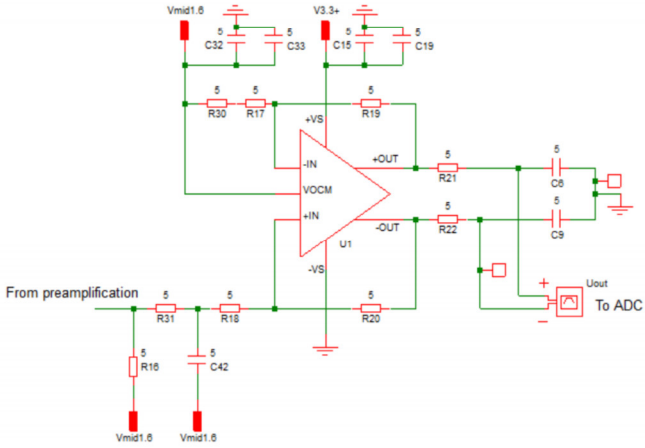

Fig. 9: Differential amplifier circuitry as realized to interface to the ADC.

In contrast, the designed analog circuitry has to provide ultra low noise over the whole useful system bandwidth, i.e. up to $B = 180\,\mathrm{MHz}$. In order to provide a more flexible signal conditioning, a programmable gain amplifier is also considered in the design.

IV. System Analysis

To analyse the system capabilities in terms of uncertainty, it is necessary to determine basic noise figures as benchmarks inflicted by the underlying electronics.

Simulations of the LNA chain suggest a spectral noise voltage of $u_{n_{sim}} = 1.75\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$ at the measurement shunt (mentioned in Sec. II). The sensor base capacitance is found from Finite Element Method (FEM) simulations to be $C_b = 109.3\,\mathrm{fF}$. The capacitance equivalent noise, which is a crucial factor for further analyses, can then be found as

$$C_n = \frac{U_n}{\frac{\partial U_{out}}{\partial C}} \tag{2}$$

It is the ratio of the input-referred noise voltage of the amplifier chain and the voltage-sensitivity of the carrier frequency

system with respect to capacitance changes. The voltage-sensitivity at the shunt resistor with respect to variations in the capacitance is

$$\frac{\partial U_{out}}{\partial C} = \frac{U_{exc}}{8C_b^2 2\pi f_c (\frac{1}{R_s} + 8\pi C_p f_c)(\frac{1}{\frac{1}{R_s}+8\pi C_p f_c} + \frac{1}{8C_b \pi f_c})^2} \tag{3}$$

where from rules for voltage dividers, we find

$$U_{out} = \frac{U_{exc} Z_p}{Z_p - (\frac{j}{2\pi f_c C_b})} \tag{4}$$

Here, a parasitic parallel capacitance $C_p = 100\,\mathrm{pF}$ (of the cable) has been included. The measurement impedance is then

$$Z_p = \frac{1}{R_s + j2\pi f_c C_p} \tag{5}$$

Subsequently, $C_n = 0.151\,\mathrm{aF}/\sqrt{\mathrm{Hz}}$ can be found. Further parameters used are the shunt resistor value of $R_s = 50\,\Omega$ (power-matched system), excitation voltage $U_{exc} = 1\,\mathrm{V}$ and carrier frequency $f_c = 20\,\mathrm{MHz}$.

We suggest the use of a calibration procedure to cope with variations in the base capacitance, uncertainties originating from topology deviations may then be neglected.

Considering a direct measurement system, we can determine the noise dependent on the bandwidth. Evaluating the sensitivity, we find that, for a position resolution of $res_{pos} \approx 50\,\mathrm{nm}$, we need to restrict the measurement bandwidth to $B = 200\,\mathrm{Hz}$. This would lead to a violation of the Nyquist criterion for the MEMS mirror resonance frequency of $f_{res} = 500\,\mathrm{Hz}$. We thus consider a parametric system description. This means, employing a system model derived from simulations, as well as prior knowledge of the mirror dynamics. Based on this model we can find a boundary for the minimum system variance with respect to system parameters. This minimum variance is known as the Cramer Rao Lower Bound (CRLB) and can be found using [21]

$$CRLB = \frac{\sigma^2}{\left(\frac{\partial s(\theta)}{\partial \theta}\right)^2} = \frac{\sigma^2}{\left(\frac{\partial C(d)}{\partial d}\right)^2} \tag{6}$$

for a signal in Additive White Gaussian Noise (AWGN). The right-hand term is an adapted version with $C(d)$ the capacitance dependent on the distance d. As was shown in [22], this leads to a system where position resolutions of $res_{pos} < 50\,\mathrm{nm}$ can well be reached. This parametric system description is subsequently suggested to be realized as EKF. The EKF is a stochastic filter algorithm providing noise reduction and position estimates of the moving mirror.

V. Results

To determine signal limitations of the analog design, we saturate the input amplifier chain to output the maximum value using a signal frequency of $f_{sig} = 1\,\mathrm{MHz}$. A Fast Fourier Transform (FFT) plot is given in Fig. 10. Obviously, there are no disturbing harmonics when the analog chain is in saturation. In Fig. 11 the respective time domain signal with maximum achievable amplitude is illustrated: The operation of the amplifier chain close to saturation leads to ripples at the upper and lower maximum of the sine curve. The signal is scaled to lie between $V_{scale} = \pm 0.5\,\mathrm{V}$ when transferred from the analog to the digital domain, the indicated achieved value of $V_{max} = 0.4995\,\mathrm{V}$ is thus close to the physical upper limit of the circuitry.

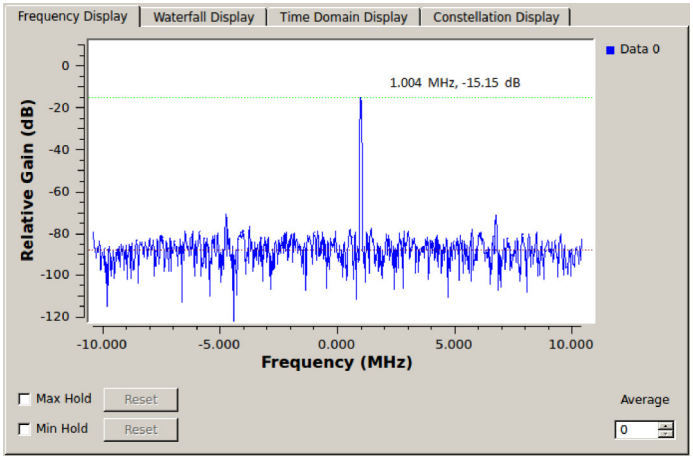

Fig. 10: FFT of an input signal with frequency $f_{sig} = 1\,\mathrm{MHz}$ (as indicated by the label).

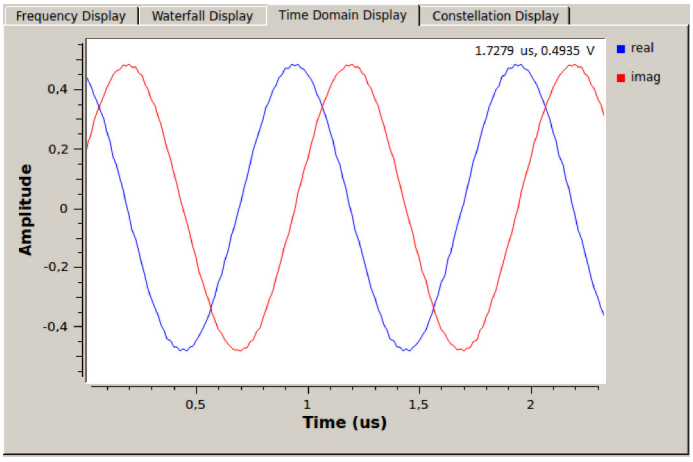

Fig. 11: Time domain signal with frequency $f_{sig} = 1\,\mathrm{MHz}$ and maximum achievable amplitude (as indicated by the label).

The noise evaluation is done for a sinusoidal input signal of $U_{in_{pp}} = 276\,\mathrm{mV_{pp}}$ or equivalently $U_{in_{eff}} = 95\,\mathrm{mV_{eff}}$ and a frequency of $f_{in} = 1\,\mathrm{MHz}$. A useful signal bandwidth of $B = 5\,\mathrm{MHz}$ is considered. The bandwidth-limitation is done for an upper corner frequency $f_{c_u} \approx 5.1\,\mathrm{MHz}$ by a high order digital filter, and for a lower corner frequency of $f_{c_l} \approx 10\,\mathrm{kHz}$ by the analog setup.

Comparing measurements of the voltage at the input and its digitized equivalent, the input-output relationship going from analog to digital domain can be found: a voltage of $u_{in} =$

$1\,\mathrm{mV}$ is mapped to a value of $u_{in_{dig}} = 0.001\,29$ in the digital domain.

Subsequently, a vector of the input signal $u_{in_{dig}}$ is recorded and subjected to an FFT. The useful signal (peak) in the FFT data is removed, to leave only noise in the spectrum. The resulting spectrum is then back-transformed (inverse FFT), yielding the noise voltage $u_{n_{out}} = 0.0023$, integrated over the used bandwidth $B = 5\,\mathrm{MHz}$. This is equivalent to a change in the effective input voltage of $\Delta U_{in_{eff}} = 1.78\,\mathrm{mV}$. To determine the noise figure Referred To the Input (RTI) $u_{n_{RTI}}$ in terms of $\mathrm{nV}/\sqrt{\mathrm{Hz}}$, it is necessary to divide $u_{n_{out}}$ by the circuit gain $G = 380$ and $\sqrt{B}$. Finally, a value of $u_{n_{RTI}} = 2.09\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$ can be found, which is in good accordance with the value of $u_{n_{sim}} = 1.75\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$ as was found in the simulation.

VI. Conclusion

In this work, design and implementation considerations for a sensor evaluation platform to be applied to a MEMS mirror system were presented. The considered hardware platform was introduced as consisting of an analog circuitry together with an FPGA and flexible signal processing software. The system topology and design were described. In the following, noise considerations were given for the developed system. Noise evaluation measurement results indicate, that the designed analog front-end is suitable as low noise input circuitry. In future work, the software building blocks on the host side, as well as the FPGA block implementation of the stochastic filter will be given.

Acknowledgement

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